Service Manual

Vol. 2

DVCPRO

DVCPRO Camera Recorder

AJ-D700P

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Sec. 2 *Schematic Diagrams*

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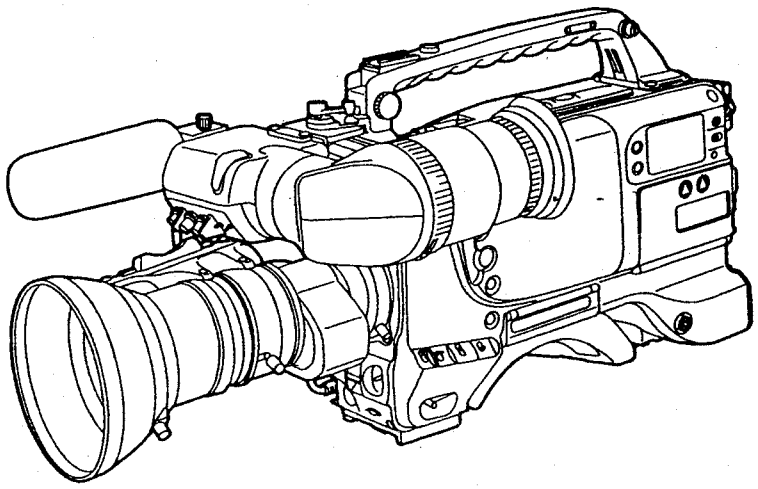

Panasonic

INTRODUCTION

This service manual contains technical information which allow service personnel to understand and service the DVCPRO Camera Recorder AJ-D700P.

Specifications

General

Power supply voltage:	DC 12 V
Power consumption:	22 W

Operating temperature:	32°F to 104°F
Storage temperature:	−4°F to 140°F
Operating humidity:	25% to 85% max. (relative humidity)
Continuous operating time:	Approx. 90 min. (using 1 Anton Bauer Trimpak 14 battery)
Weight:	Approx. 12.76 lbs (5.8 kg) (incld. main unit, viewfinder, lens, battery pack and tape)
Dimensions:	

Camera Section

Pick-up devices:	1/2-inch on-chip FIT type of CCD
System:	RGB 3-CCD system
Picture elements:	410,000 pixel
Spectrum system:	F1.4 prism system
Built-in filters:	1; 3200K 2; 5600K+1/4 ND 3; 5600K 4; 5600K+1/16 ND
Quantization:	10-bit A/D (R, G and B channels), 14.3 MHz
Digital signal processing:	16-bit long operation, 14.3 MHz/28.6 MHz
Programmable gains:	3 positions can be set from among −3, 0, 3, 6, 9, 12, 15, 18, 21, 24 and 30 dB.
Shutter speeds:	1/100, 1/120, 1/250, 1/500, 1/1000 and 1,2000 sec. Synchro scan mode; 1/30.4−1/57.4 sec., 1/61.7−1/250 sec.
Lens mount:	1/2" Bayonet type
Sensitivity:	F8(2000Lux, 89.9% reflection)
Minimum subject brightness:	2Lux (F1.4+30 dB)
Image S/N ratio:	62 dB (typ.)
Horizontal resolution:	750 TV lines (typ.)
Vertical resolution:	400 TV lines/450 TV lines (SUPER V) (typ.)
Registration:	Below 0.05% (entire range) (excld. lens)
Geometric distortion:	Below measurable limit (excld. lens)

Viewfinder

CRT:	1.5 type monochrome
Resolution:	600 TV lines

Specifications

VTR Video System (during playback on a standard playback unit)

Bands:	Brightness; 0 Hz to 5.75 MHz +1.0 dB/−3.0 dB
S/N ratio:	55 dB
K factor (2T pulse):	Within 2%
Linearity:	Within 2%
Y/C delay:	Within 20 ns

VTR Audio System (during playback on a standard playback unit)

Sampling frequency:	48 kHz (synchronized to video)
Quantization:	16-bits/sample
Frequency response:	20 Hz to 20 kHz±1.0 dB (at reference level)
Dynamic range:	85 dB or more (at 1 kHz, AWTD)
Distortion:	Within 0.1% (at 1 kHz, operating level)
Wow/flutter:	Below measurable limit
Head room:	20 dB
Emphasis:	T1=50 µs, T2=15 µs (can be turned ON/OFF)

VTR Tape Running System

Tape speed:	33.813 mm/s
Recording/playback time:	63 min. (using the AJ-P63M)
FF/REW time:	Approx. 3 min.(using the AJ-P63M)

Connectors

Input

AUDIO IN CH1/CH2 (XLR, 3-pin, male):	MIC/LINE switchable MIC; Menu setting to −60/−50/−40 dBu LINE; Menu setting to −6/0/+4 dBu
MIC IN (XLR, 3-pin, female):	Menu setting to −60/−50/−40 dBu, balanced 3 kohm
GENLOCK IN (BNC):	1.0 Vp-p, 75 ohm
TIME CODE IN (12-pin):	0.5 to 18 Vp-p, 10 kohm

Output

CAMERA OUT (BNC):	1.0 Vp-p, 75 ohm
VIDEO OUT (BNC):	1.0 Vp-p, 75 ohm
AUDIO OUT (XLR, 3-pin, female):	+4 dBu, balanced, low-impedance (Menu setting to CH1/CH2/MIX)
AUDIO CH1/CH2 OUT (12-pin, TC IN/OUT combined):	−20 dBu, unbalanced, low-impedance
VTR (26-pin, option):	
TIME CODE OUT (12-pin):	1.0 Vp-p, 75 ohm
PHONES (mini-jack×2):	

Other

DC IN (XLR, 4-pin, male):	DC 11 to 17 V
DC OUT (4-pin):	DC 11 to 17 V, maximum rated.current; 0.1 A
LENS (12-pin):	
REMOTE (ECU, 6-pin):	

Accessories

Shoulder belt (1)
Sony battery connector, NP-1 screw
26P Output adaptor (1)

Weight and dimensions shown are approximate.
Specifications are subject to change without notice.

Power supply related

AU-BP220, AU-BP402 battery packs
AG-B425 battery charger (for charging the AU-BP220 and AU-BP402 battery packs)
AU-M402 battery case
AU-B110 AC adaptor

Video cassette tapes

AJ-P6MP, AJ-P12MP, AJ-P23MP, AJ-P33MP, AJ-P63MP metal tapes

Viewfinder

5-inch viewfinder

External VTR-related

AU-55H, AG-7450A portable video cassette recorders
AG-S745 VTR adaptor (for connecting the AG-7450A portable VTR)
AJ-YA700P 26-pin output connector (for connecting an external VTR to the 26-pin interface)
Connection cables
- for connecting an external VTR to the 26-pin interface
- for connecting an external VTR to the 14-pin/26-pin interface

AQ-EC1 extension control unit

Audio components

SHAN-MC700P microphone kit
Stereo microphone
AJ-MH700P microphone holder
WX-RA700 wireless receiver
WX-R980 camera attachment

Maintenance products

AJ-CL12MP cleaning tape
AJ-SC700 soft carrying case
SHAN-RC700 rain cover (complementary)

SAFETY PRECAUTIONS

GENERAL GUIDELINES

1. When servicing, observe the original lead dress. If a short circuit is found, replace all parts which have been overheated or damaged by the short circuit.
2. After servicing, see to it that all the protective devices such as insulation barriers, insulation papers shields are properly installed.
3. After servicing make the following leakage current checks to prevent the customer from being exposed to shock hazards.

LEAKAGE CURRENT COLD CHECK

1. Unplug the AC cord and connect a jumper between the two prongs on the plug.
2. Measure the resistance value, with an ohm meter, between the jumpered AC plug and each exposed metallic cabinet part on the equipment such as screwheads, connectors, control shafts, etc. When the exposed metallic part has a return path to the chassis, the reading should be between 1 MΩ and 5.2MΩ .
   When the exposed metal dose not have a return path to the chassis, the reading must be ∞ .

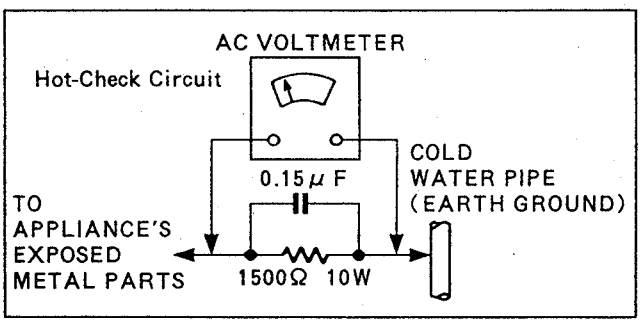

Figure 1

LEAKAGE CURRENT HOT CHECK (See Figure 1)

1. Plug the AC cord directly into the AC outlet.
   Do not use an isolation transformer for this check.
2. Connect a 1.5KΩ , 10W resistor, in parallel with 0.15μ F capacitor, between each exposed metallic part on the set an a good earth ground such as a water pipe, as shown in Figure 1.
3. Use an AC voltmeter, with 1000 ohms/volt or more sensitivity, to measure the potential across the resistor.
4. Check each exposed metallic part, and measure the voltage at each point.
5. Reverse the AC plug in the AC outlet repeat each of the above measurements.
6. The potential at any point should not exceed 0.75 volts RMS. A leakage current tester (Simpson Model 229 equivalent) may be used to make the hot checks, leakage current must not exceed 1/2 milliamp. In case a measurement is outside of the limits specified, there is a possibility of a shock hazard, and the equipment should be repaired and rechecked before it is returned to the customer.

ELECTROSTATICALLY SENSITIVE (ES) DEVICES

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically sensitive (ES) Devices. Examples of typical ES devices are integrated circuits and some field-effect transistors and semiconductor "chip" components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground.
   Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ES devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded tip soldering iron to solder or unsolder ES devices.
4. Use only an anti-static solder removal device classified as "anti-static" can generate electrical charges sufficient to damage ES devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ES devices.
6. Do not remove a replacement ES device from its protective package until immediately before you are ready to install it. (most replacement ES devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive material).
7. Immediately before removing the protective material from the leads of replacement ES device, touch the protective material to the chassis or circuit assembly into which the device will be installed.
   CAUTION: Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.
8. Minimize bodily motions when handling unpackaged replacement ES devices. (Otherwise harmless mother such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ES device).

X-RADIATION

WARNING

1. The potential source of X-Radiation in EVF sets is the High Voltage section and the picture tube.
2. When using a picture tube test jig for service, ensure that jig is capable of handling 10kV without causing X-Radiation.

NOTE: It is important to use an accurate periodically calibrated high voltage meter.

3. Measure the High Voltage. The meter (electric type) reading should indicate 2.5kV, ± 0.15kV. If the meter indication is out of tolerance, immediate service and correction is required to prevent the possibility of premature component failure. To prevent an X-Radiation possibility, it is essential to use the specified picture tube.

SECTION 1

BLOCK DIAGRAMS

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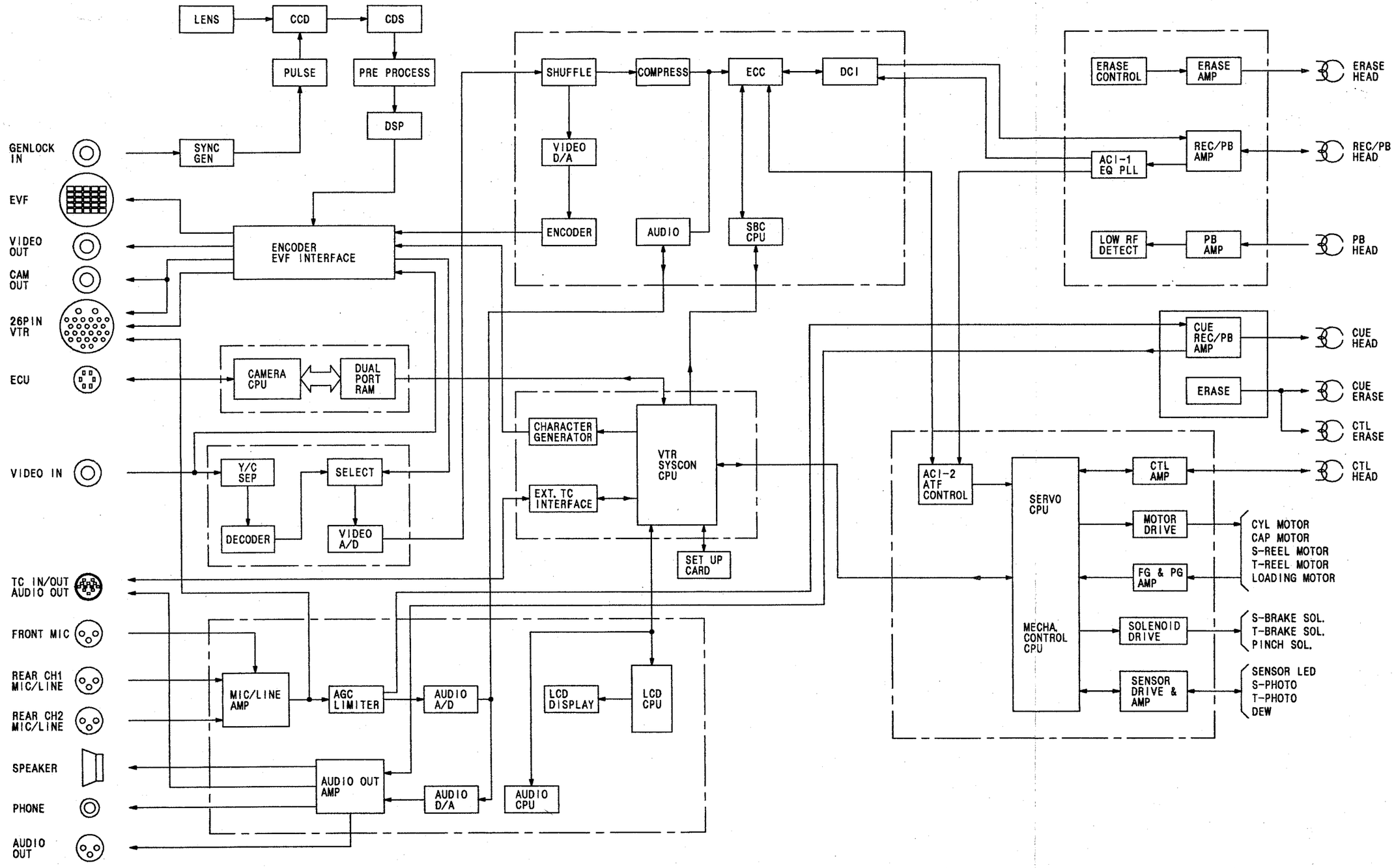
OVERALL BLOCK DIAGRAM



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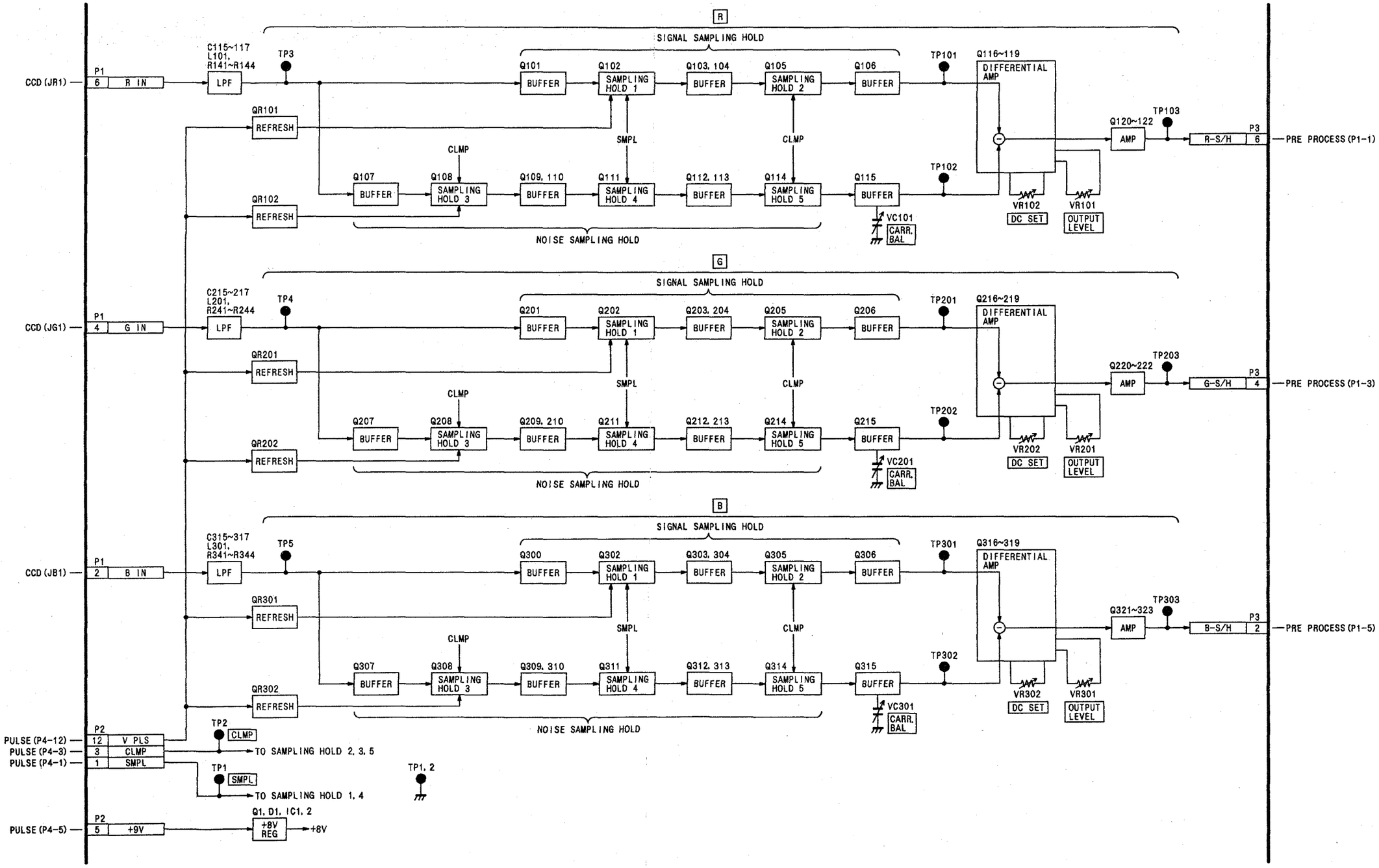
CDS BLOCK DIAGRAM



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CDS P.C.Board

CDS is the abbreviation of Correlated Double Sampling which smoothes CCD outputs.

Input signal, **R IN,** from CCD P.C.Board is processed with **LPF.** After that it has two ways. Upper one is for signal component process, lower one is for noise component.

In upper way the sample pulse,**SMPL,** samples and holds the charge level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of signal component.

In lower way the sample pulse,**SMPL,** samples and holds the noise level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of noise component.

The difference between signal component and noise component is output to Pre Process P.C.Board as **R-S/H.**

VC101 is the VR to minimize career leak. **VR102** adjusts DC level, and **VR101** does output level.

Input signal, **G IN,** from CCD P.C.Board is processed with **LPF.** After that it has two ways. Upper one is for signal component process, lower one is for noise component.

In upper way the sample pulse,**SMPL,** samples and holds the charge level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of signal component.

In lower way the sample pulse,**SMPL,** samples and holds the noise level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of noise component.

The difference between signal component and noise component is output to Pre Process P.C.Board as **G-S/H.**

VC201 is the VR to minimize career leak. **VR202** adjusts DC level, and **VR201** does output level.

Input signal, **B IN,** from CCD P.C.Board is processed with **LPF.** After that it has two ways. Upper one is for signal component process, lower one is for noise component.

In upper way the sample pulse,**SMPL,** samples and holds the charge level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of signal component.

In lower way the sample pulse,**SMPL,** samples and holds the noise level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of noise component.

The difference between signal component and noise component is output to Pre Process P.C.Board as **B-S/H.**

VC301 is the VR to minimize career leak. **VR302** adjusts DC level, and **VR301** does output level.

Pulse P.C.Board

This circuit makes those pulses which drive CCD.

IC2 makes V-CCD Drive Pulse of **VA1～VA4,VB1～VB4**,Charge Pulse of **CH1,CH2** and Shutter Pulse of **CHS** from V Drive Pulse **CCD VD** supplied from Sync P.C.Board. Shutter speed is controlled by **SHUT A,SHUT B** and **SHUT C.** The logic table is located on the top left of the diagram.

SLOW SHUTTER of **IC7,IC8** and **IC9** make the shutter pulse used in 1/50 of shutter speed. V-CCD Drive Pulses are supplied to CCD P.C.Board as **XVA1～XVA2, XVB1～XVB4.**

VR14 can shift H Drive, **CCD HD,** to change moduration.

The PLL which is composed of phase comparator in **IC2** and oscillator **X1** generates H-CCD Drive Pulse **H12** and **H34** in **IC1** locked to **CCD HD.** These are supplied to CCD P.C.Board as **XH1, XH2.**

Reset Pulse of**XR**, Clamp Pulse of **CLMP** and Sample Pulse of **SMPL** are generated in the same way and supplied to CCD P.C.Board.

OG Voltage of R/G/B depend on **VR10,VR11** and **VR12.** SUB Voltage depend on **VR7,VR8** and **VR9.**

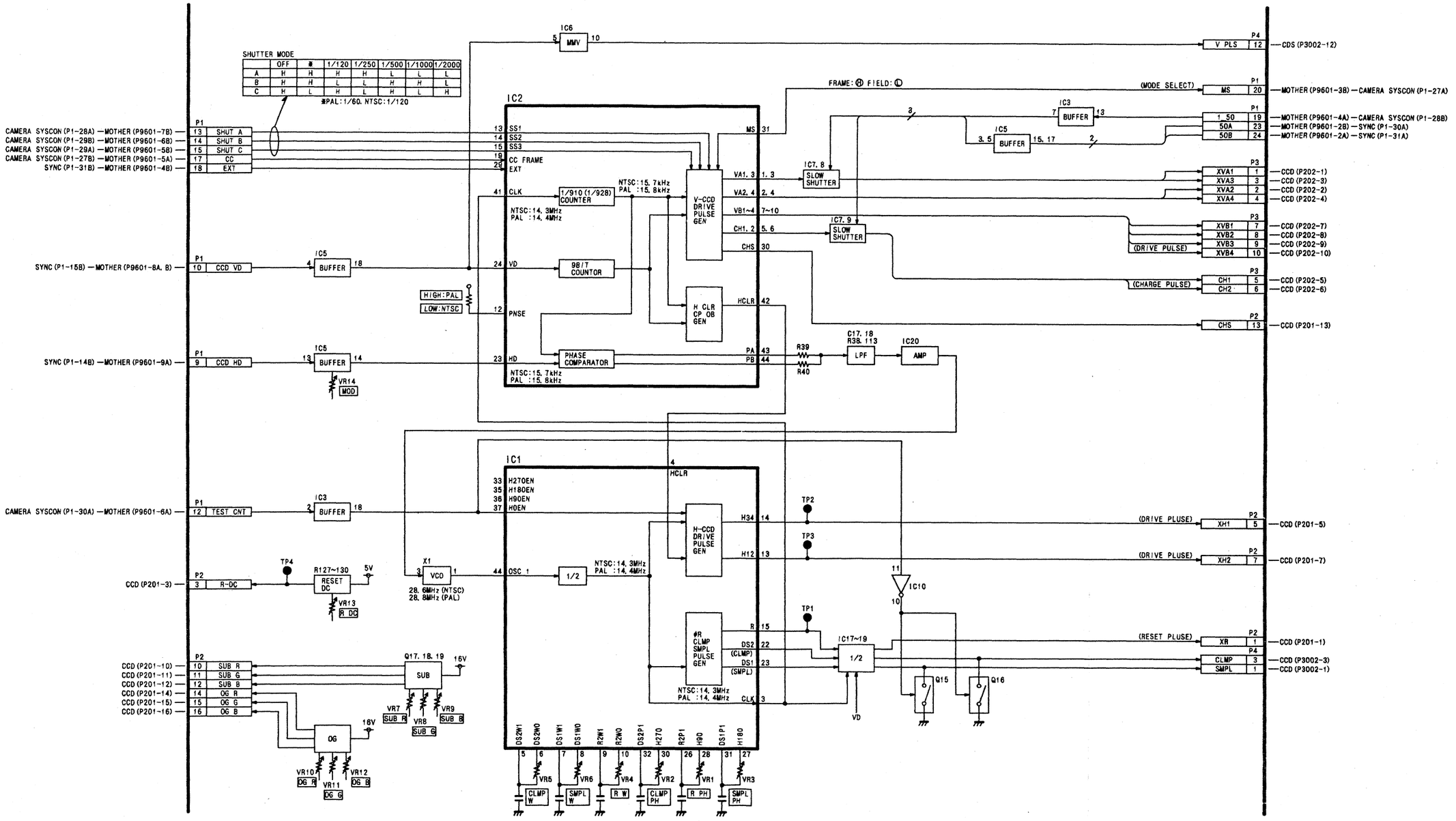
The width and phase of Sample Pulse are adjusted with **VR6** and **VR3.**

The width and Phase of Clamp Pulse are adjusted with **VR5** and **VR2.**

The width and Phase of Reset Pulse are adjusted with **VR4** and **VR1.**

DC voltage of Reset Pulse is adjusted with **VR13.**

PULSE BLOCK DIAGRAM



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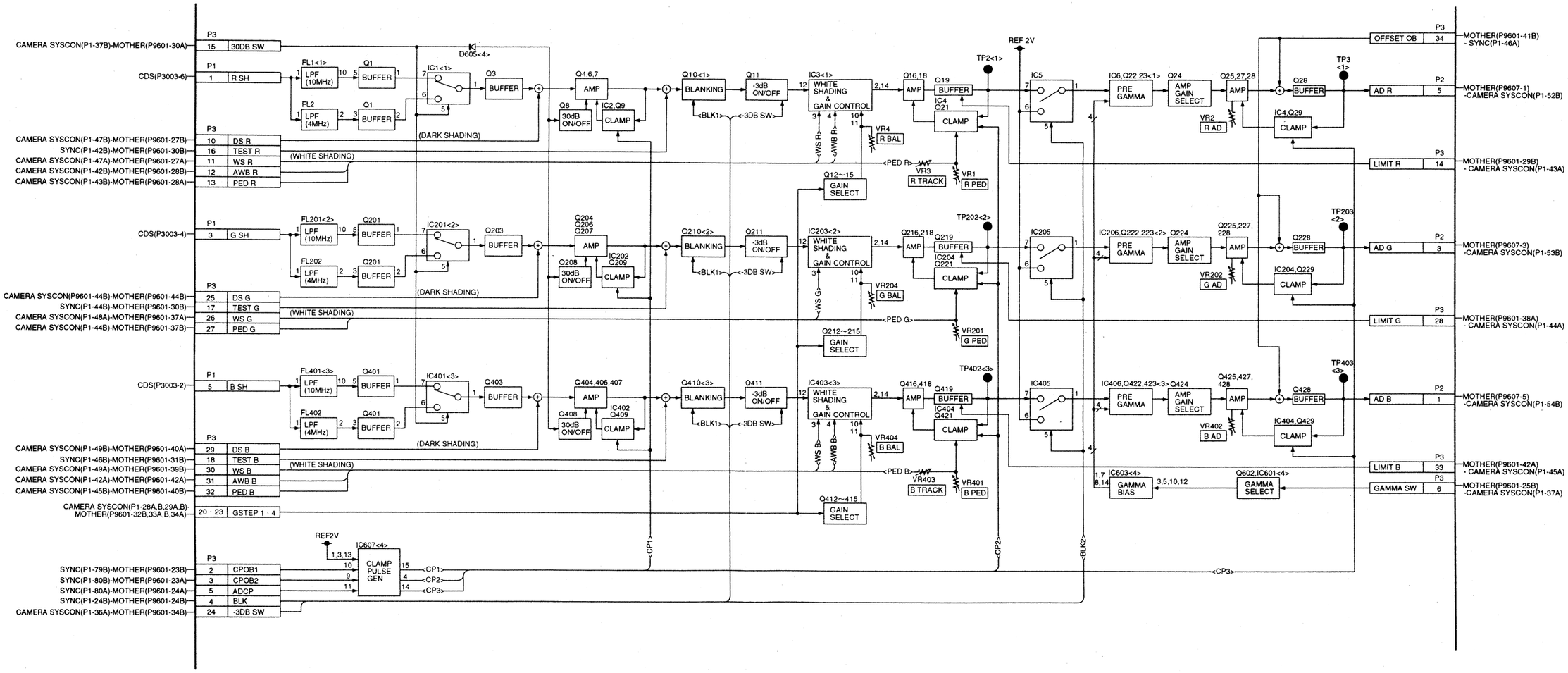
PRE PROCESS BLOCK DIAGRAM



1—6

Pre Process P.C.Board

This circuit processes Dark Shading, White Shading, Pre Gamma and so on.

R S/H supplied from CDS P.C.Board is input to LPF,**FL1.** Another filter **FL2** thins reset pulses to read two pixels together when GAIN is set to 30dB. **IC1** is a switch prepared for this function. It selects 6th pin side in 30dB mode, otherwise does 7th pin. The switching signal is **30DB SW** supplied to 5th pin.

Dark Shading,**DS R,** is added to the output from **IC1.** The signal is adjusted in Gain at **Q4, 6 and 7** and selected with **TEST R** which is a RAMP signal for test.

IC3 processes White Shading,**WS R,** and Auto White Balance,**AWB R. VR1** adjusts pedestal level. **VR3** adjusts pedestal tracking.

IC5 processes Blanking. **IC6, Q22** and **Q23** process Pre Gamma. **VR2** adjusts the level required before A/D conversion. Finally the signal is output to DSP P.C.Board as **AD R.**

G S/H supplied from CDS P.C.Board is input to LPF,**FL201.** Another filter **FL202** thins reset pulses to read two pixels together when GAIN is set to 30dB. **IC201** is a switch prepared for this function. It selects 6th pin side in 30dB mode, otherwise does 7th pin. The switching signal is **30DB SW** supplied to 5th pin.

Dark Shading,**DS G,** is added to the output from **IC201.** The signal is adjusted in Gain at **Q204, 206 and 207** and selected with **TEST G** which is a RAMP signal for test.

IC203 processes White Shading,**WS G,** and Auto White Balance,**AWB G. VR201** adjusts pedestal level.

IC205 processes Blanking. **IC206, Q222** and **Q223** process Pre Gamma. **VR202** adjusts the level required before A/D conversion. Finally the signal is output to DSP P.C.Board as **AD G.**

B S/H supplied from CDS P.C.Board is input to LPF,**FL401.** Another filter **FL402** thins reset pulses to read two pixels together when GAIN is set to 30dB. **IC401** is a switch prepared for this function. It selects 6th pin side in 30dB mode, otherwise does 7th pin. The switching signal is **30DB SW** supplied to 5th pin.

Dark Shading,**DS B,** is added to the output from **IC401.** The signal is adjusted in Gain at **Q404, 406 and 407** and selected with **TEST B** which is a RAMP signal for test.

IC403 processes White Shading,**WS B,** and Auto White Balance,**AWB B. VR401** adjusts pedestal level. **VR403** adjusts pedestal tracking.

IC405 processes Blanking. **IC406, Q422** and **Q423** process Pre Gamma. **VR402** adjusts the level required before A/D conversion. Finally the signal is output to DSP P.C.Board as **AD B.**

CCD P.C.Board

This Board has three CCDs and CCD drive circuits for RGB processes.

IC101 and **IC102** make the drive pulses for R CCD.

XVA1~4 generated in Pulse P.C.Board are input to **IC101**. Those pulses become V-CCD Drive Pulses for image area **(A1R~A4R)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V).

XVB1~4 generated in Pulse P.C.Board are input to **IC102.** Those pulses become V-CCD Drive Pulses for storage area **(B1R~B4R)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V). **A1R~A4R** and **B1R~B4R** are supplied to **IC103,R CCD**.

CH1 and **CH2** are charge pulses and added to V-CCD Drive Pulses for image area. **CHS** is shutter pulse and becomes a pulse of 21V in **IC101**. This is added to SUB voltage, **SUB R,** and supplied to **IC103, R CCD**. H-CCD Drive Pulses, **H1R** and **H2R,** are generated in **IC208** from **XH1** and **XH2** and supplied to **IC103, R CCD**. Reset Pulse is generated in **IC207** from **XR** and **R DC** and supplied to **IC103, R CCD**. The output signal from **R CCD** is supplied to CDS P.C.Board via connector **JR**.

IC201 and **IC202** make the drive pulses for G CCD.

XVA1~4 generated in Pulse P.C.Board are input to **IC201**. Those pulses become V-CCD Drive Pulses for image area **(A1G~A4G)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V).

XVB1~4 generated in Pulse P.C.Board are input to **IC202.** Those pulses become V-CCD Drive Pulses for storage area **(B1G~B4G)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V). **A1G~A4G** and **B1G~B4G** are supplied to **IC203,G CCD**.

CH1 and **CH2** are charge pulses and added to V-CCD Drive Pulses for image area. **CHS** is shutter pulse and becomes a pulse of 21V in **IC201**. This is added to SUB voltage, **SUB G,** and supplied to **IC203, G CCD**. H-CCD Drive Pulses, **H1G** and **H2G,** are generated in **IC208** from **XH1** and **XH2** and supplied to **IC203, G CCD**. Reset Pulse is generated in **IC207** from **XR** and **R DC** and supplied to **IC203, G CCD**. The output signal from **G CCD** is supplied to CDS P.C.Board via connector **JG**.

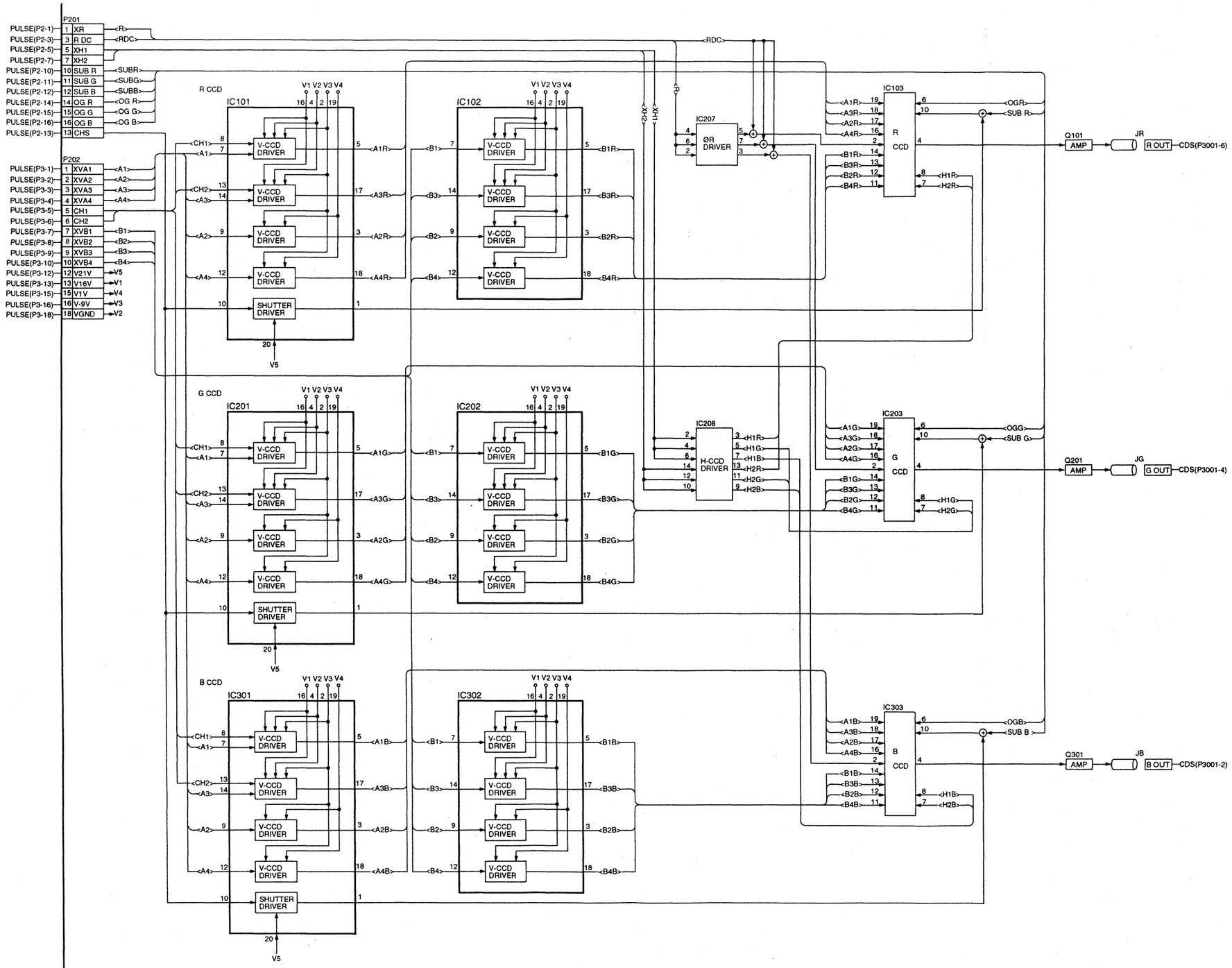
IC301 and **IC302** make the drive pulses for B CCD.

XVA1~4 generated in Pulse P.C.Board are input to **IC301**. Those pulses become V-CCD Drive Pulses for image area **(A1B~A4B)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V).

XVB1~4 generated in Pulse P.C.Board are input to **IC302.** Those pulses become V-CCD Drive Pulses for storage area **(B1B~B4B)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V). **A1B~A4B** and **B1B~B4B** are supplied to **IC303,B CCD**.

CH1 and **CH2** are charge pulses and added to V-CCD Drive Pulses for image area. **CHS** is shutter pulse and becomes a pulse of 21V in **IC301**. This is added to SUB voltage, **SUB B,** and supplied to **IC303, B CCD**. H-CCD Drive Pulses, **H1B** and **H2B,** are generated in **IC208** from **XH1** and **XH2** and supplied to **IC303, B CCD**. Reset Pulse is generated in **IC207** from **XR** and **R DC** and supplied to **IC303, B CCD**. The output signal from **B CCD** is supplied to CDS P.C.Board via connector **JB**.

CCD BLOCK DIAGRAM



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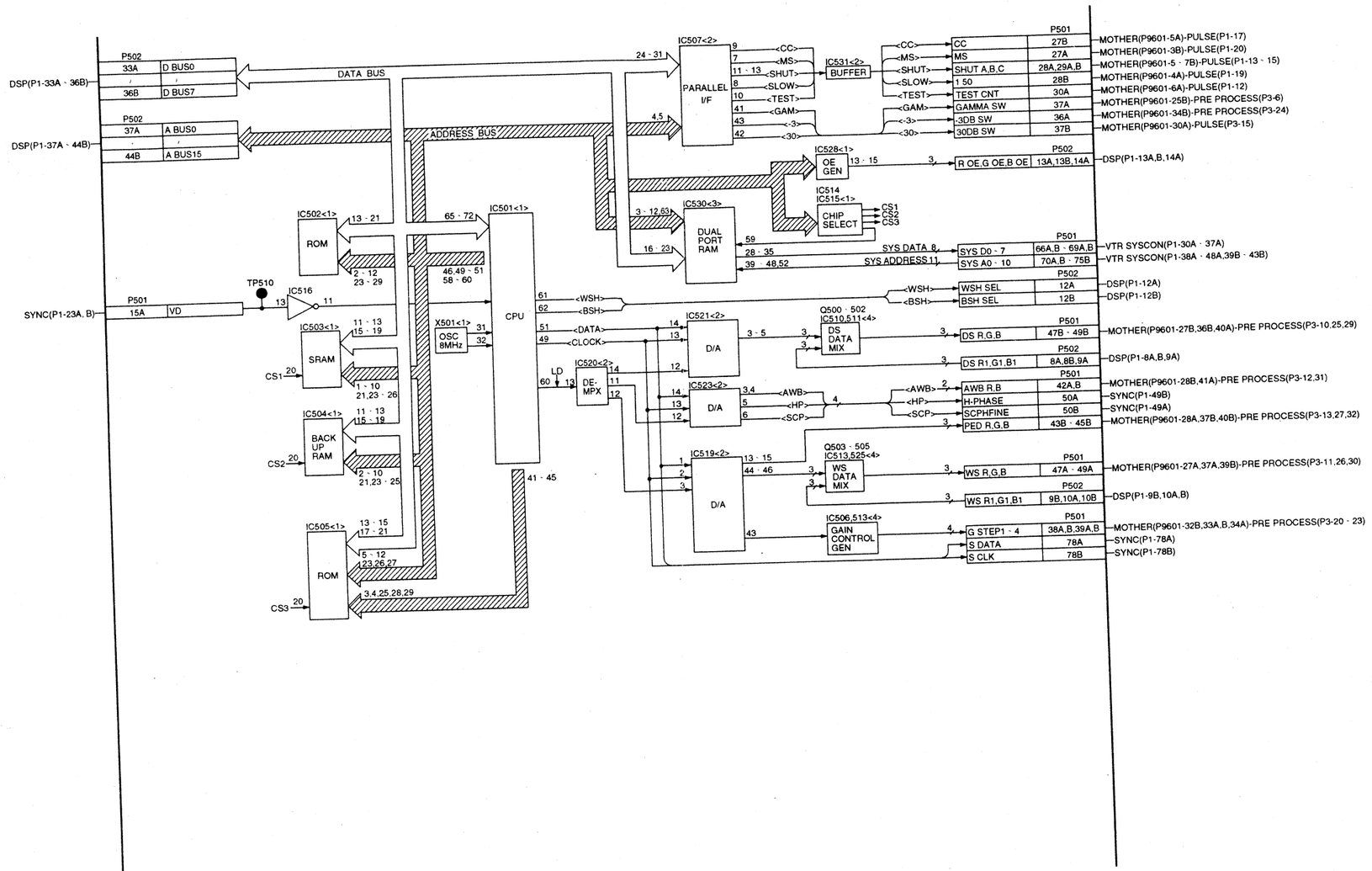
CAMERA SYSCON BLOCK DIAGRAM



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Camera Syscon P.C.Board

This circuit which is composed of following ICs controls Camera unit and EVR.

IC501	SYSCON CPU
IC502	SYSCON ROM
IC504	Back-up RAM
IC507	Parallel I/F to change Mode
IC530	Dual Port RAM for communication with VTR SYSCON

IC521 is D/A converter for Dark Shading data. This is supplied to **DS DATA MIX** which is composed of **Q500 ~ Q502, IC510** and **IC511**. The data is added to RGB of **DS R1,G1,B1** and output as **DS R,G,B**.

IC519 is D/A converter for White Shading data. This is supplied to **WS DATA MIX** which is composed of **Q503 ~ Q505, IC513** and **IC525**. The data is added to RGB of **WS R1,G1,B1** and output as **WS R,G,B**.

The data of AWB, H phase and sub-carrier are D/A converted at **IC523**. Each of those is output as **AWB ,R B, H-PHASE** and **SCPHASE**.

DSP P.C.Board

DSP is the abbreviation of Digital Signal Processor and processes Blemish Compensation, Gamma, Knee, Masking, Detail and so on at **IC101** and **IC102.**

AD R,AD G and **AD B** supplied from Pre Process P.C.Board are A/D converted to 10bits of parallel signals at **IC4,IC5** and **IC6. VR1** adjusts the reference voltage for A/D conversion. R,G, and B converted to digital signal are supplied to **IC101.** On the other hand Dark Shading data is supplied to **IC301,SRAM,** via **IC302** and **IC305**. White Shading data is also supplied to **IC304,SRAM,** via **IC302** and **IC305.** Both are D/A converted at **IC303** and **IC306** and then supplied to Camera Syscon P.C.Board.

R, G, B input to **IC101** are processed with Blemish Compensation, Gamma, Knee and Masking. Then they are supplied to **IC102.** At the same time the detail signal made inside **IC101** are processed with Level Dependent, Dynamic Noise Suppress and Dynamic Detail at **IC102.**

1/2 pitch of CCD spatial offsets is compensated in **IC102.** Moreover Chroma Detail and Fresh(Skin) Detail are produced from R,G and B and then added to R,G and B as well as ordinary details mentioned above.

The multiplexers after 1/2 pitch of CCD spatial offsets compensation switch input signal or internal color bar.

After that Clipping and Blanking are performed.

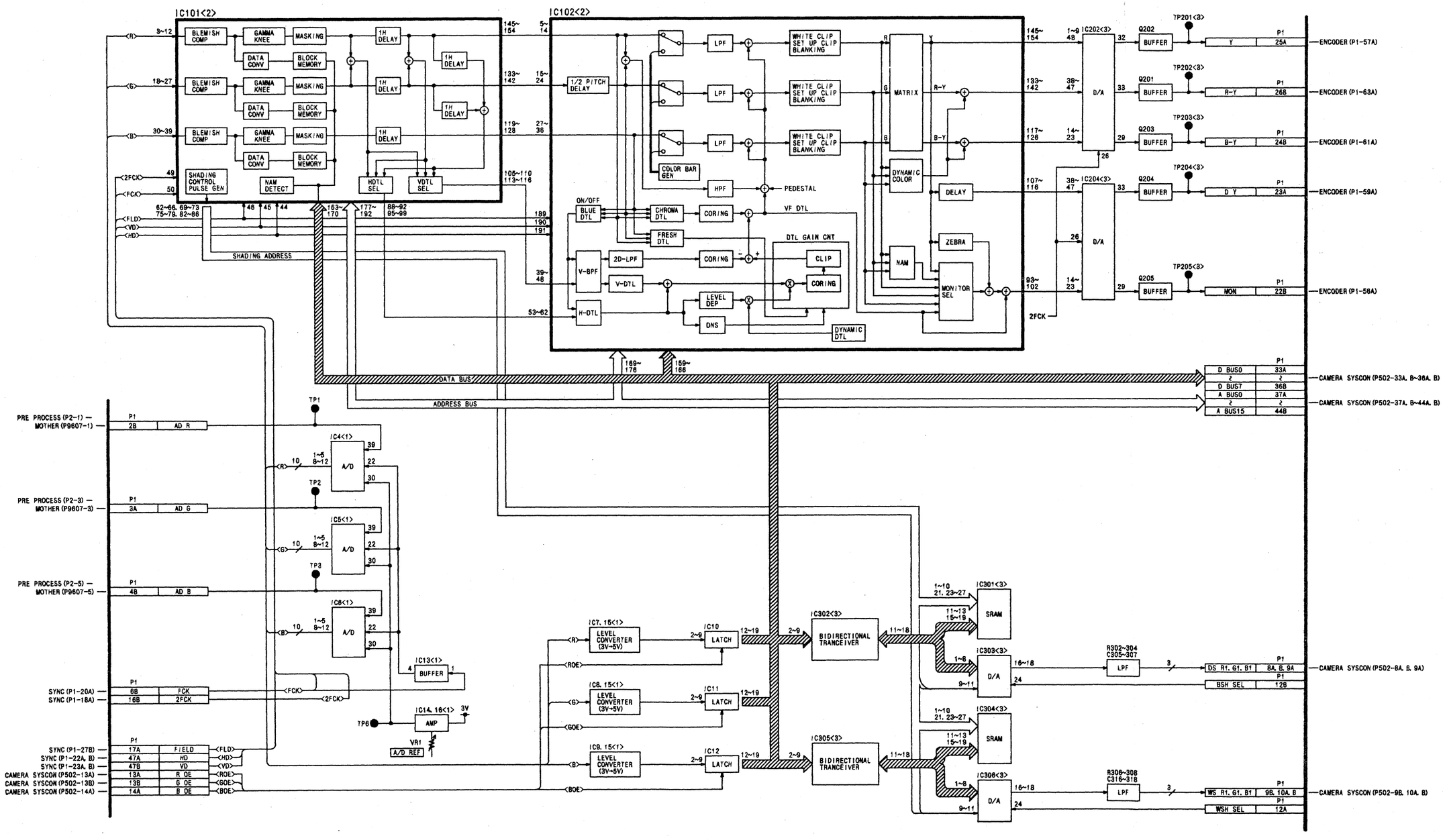
MATRIX converts **RGB** to **Y/R-Y/B-Y**.

Outputs from **145th~154th** pins are **Y, 133th~142nd** pins are **R-Y,** and **117th~126th** pins are **B-Y.** All of those are converted to analog signals at **IC202** and supplied to Encoder P.C.Board.

D Y output from **107th~116th** pins are delayed Y signal which is required to encode composite signal in Encoder P.C.Board.

Outputs from **93th~102nd** pins are Y,R,G,B or NAM for EVF which have ZEBRA. This is converted to analog signal at **IC204** and supplied to Encoder P.C.Board.

DSP BLOCK DIAGRAM



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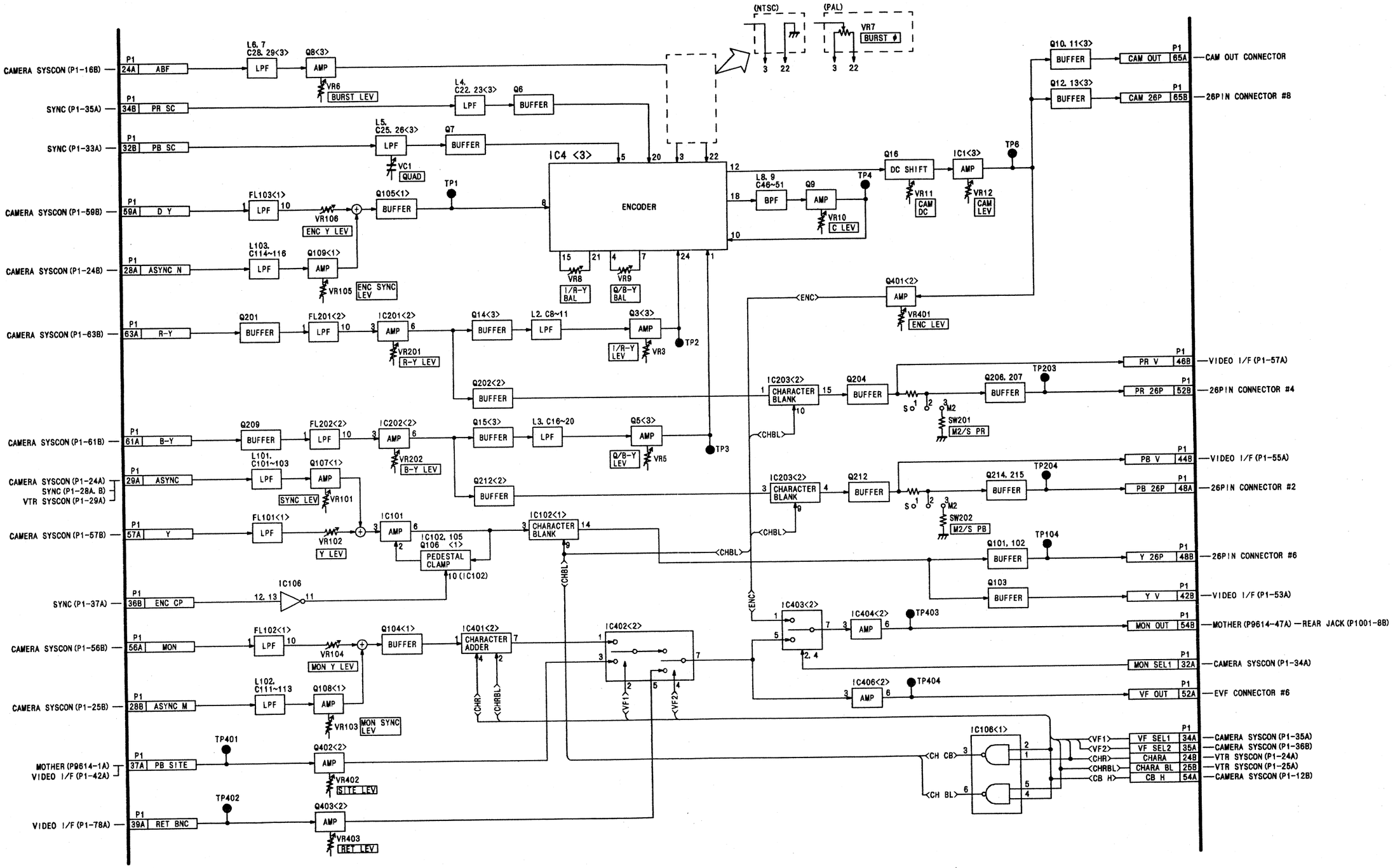
ENCODER BLOCK DIAGRAM



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Encoder P.C.Board

Encoder converts inputs from DSP to composite and component signals.

IC4 is an encoder. **D Y**(Y for composite) is input to **8th** pin, **R-Y** to **24th** pin, and **B-Y** to **1st** pin.

VR106 adjusts the level of **D Y.** Sync. **ASYNC N** is added to **D Y. D Y** goes to **IC4. VR105** adjusts the level of sync.

R-Y is adjusted in level with **VR201** and supplied to **IC4.** On the other hand it is output as Pr signal **PR V**, **PR 26P. PR V** is to be recorded in AJ-D700. **PR 26P** is to be output via 26 pins connector(Option).

SW201 selects M2 level or β cam level for 26 pins connector.

B-Y is adjusted in level with **VR202** and supplied to **IC4.** On the other hand it is output as Pb signal **PB V**, **PB 26P. PB V** is to be recorded in AJ-D700. **PB 26P** is to be output via 26 pins connector(Option).

SW202 selects M2 level or β cam level for 26 pins connector.

Sub-carriers are supplied to **IC4** as **PR SC** and **PB SC. ABF** is Burst signal and is adjusted in level with **VR6.**

R-Y and B-Y are modulated to C signal at **IC4. VR10** adjusts the C level. C signal returns to **IC4** and encoded with Y. Mixed signal is output from **12th** pin. After DC(**VR11**) and level(**VR12**) are adjusted, composite signal has three ways; **CAM OUT, CAM 26P** for 26 pins connector, **MON OUT** for VIDEO OUT connector. **VR401** adjusts the level of **MON OUT.**

VR102 adjusts the level of ordinary **Y.** Then sync., **ASYNC,** is added to **Y. VR101** adjusts the level of sync. After pedestal is added at **IC101, Y** is output as **Y V** and **Y 26P. Y V** is to be recorded in AJ-D700. **Y 26P** is to be output via 26 pins connector(Option).

MON is Y,R,G,B or NAM for EVF and is adjusted in level with **VR104.** Sync.,**ASYNC M,** is added to that signal. Sync level is adjusted with **VR103. IC401** adds superimpose. **IC402** selects **PB SITE** for playback or **RET BNC** for Return. After that the signal is supplied to EVF as **VF OUT.** On the other hand **IC403** selects VF signal or composite signal for VIDEO OUT connector at **IC403.** The selected signal is supplied to Rear Jack P.C.Board as **MON OUT.**

VR402 adjusts the level of PB signal.

VR403 adjusts the level of RETURN input.

Sync. P.C.Board

This circuit is composed of **IC27** and **IC11**.

GL IN is input from GEN LOCK IN connector. Composite sync. separated at **IC34** is supplied to **98th** pin of **IC27** and **85th** pin of **IC11**. Burst signal is separated at **IC2** and **IC3** and supplied to **69th** pin of **IC27**. H SYNC. is separated from the sync. input from **98th** pin of **IC27**. Then H SYNC. is output from **101st** pin. This is adjusted in phase at **IC22** and input again from **43th** pin.

X4 located at left side of diagram generates reference 4FSC. H sync. is generated based on that 4FSC. This H sync. or **HR**, external input sync. input from **45th** pin is selected at **IC27**. Selected signal is output from **46th** pin as **HO**. **X1** located at top of diagram generates **2FCK** locked to **HO** and then supplied to **IC11**.

IC11 generates clocks which is used in camera unit and locked to that **2FCK**.

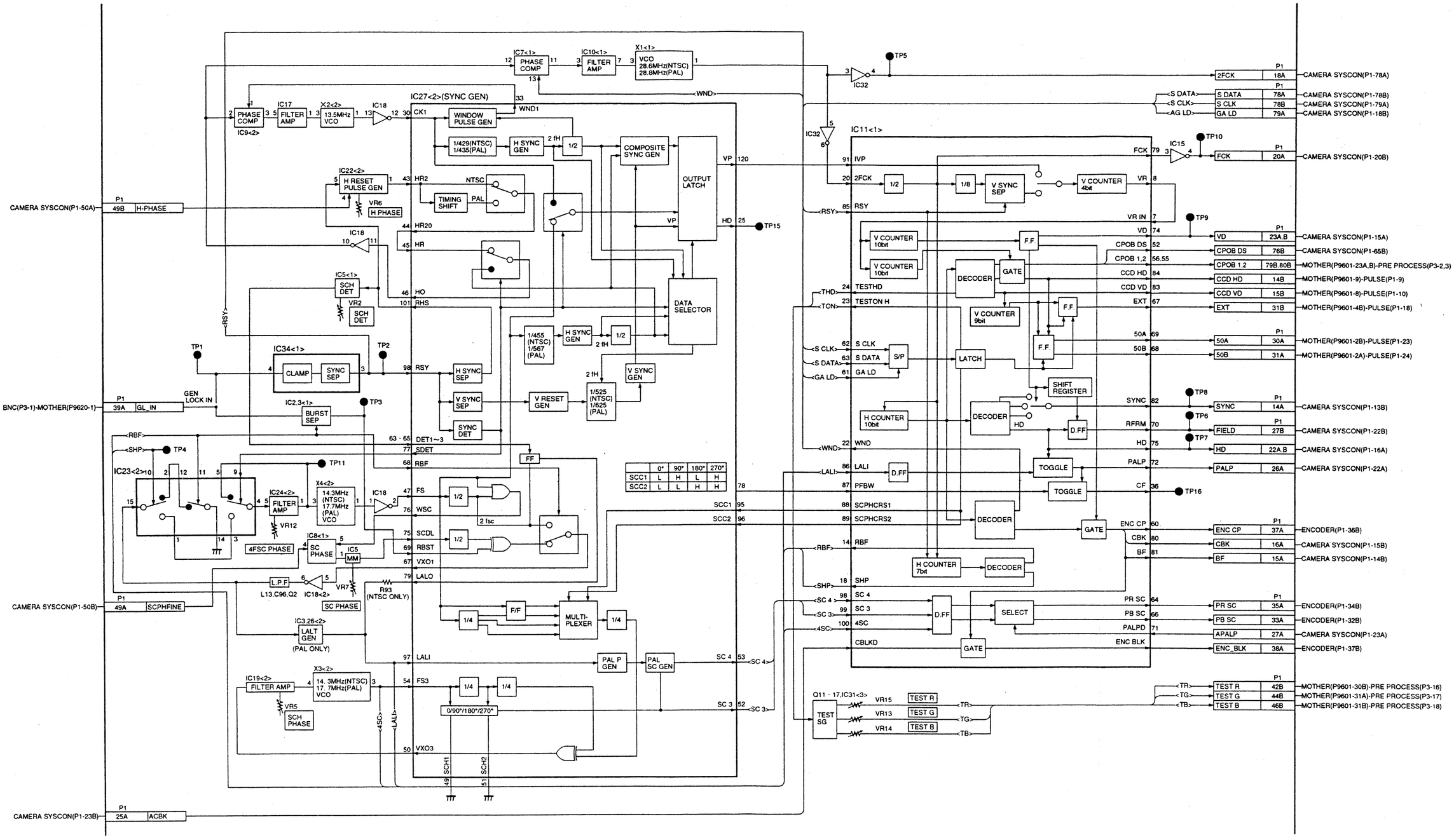
PLL located at top left of diagram which is composed of **IC9** of phase comparator and **X2** of 13.5MHz oscillator drives **IC27**.

PLL located at bottom left of diagram which is composed of **IC19** of phase comparator and **X3** of oscillator adjusts SCH.

The signals at **95th** and **96th** pins of **IC27** are used for sub-carrier adjustment.

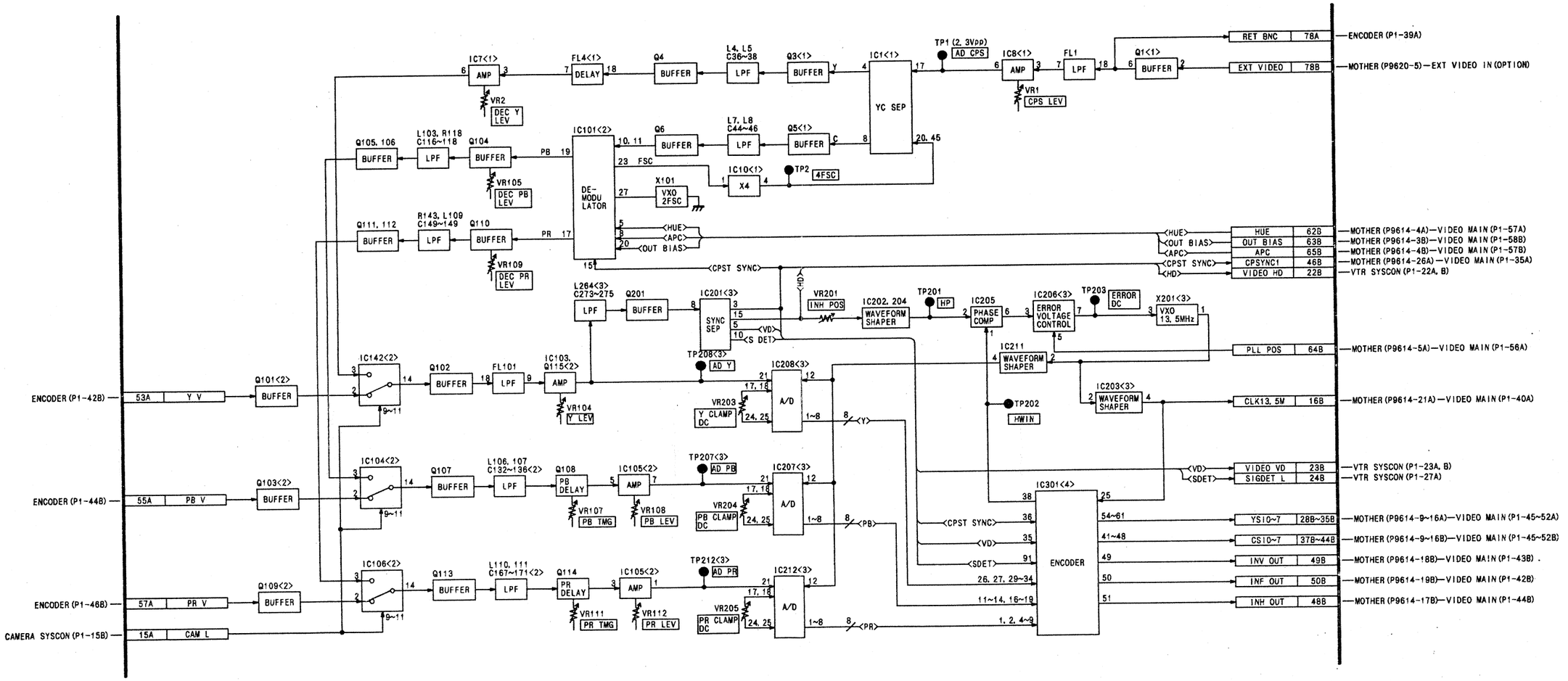
Q11~Q17 and **IC31** generate Ramp signal for testing which is adjusted in level with **VR13~VR15**.

CAMERA SYNC BLOCK DIAGRAM



1—17

VIDEO I/F BLOCK DIAGRAM



1—18

Video I/F P.C.Board

VIDEO I/F is the interface between camera unit and VTR unit.

EXT VIDEO is external video input from VIDEO IN connector. This is supplied to Encoder as Return signal, **RET BNC** , and also supplied to **IC1** for Y/C separation after level adjustment with **VR1**. Y is adjusted in level with **VR2** and supplied to **IC142**. C is demodulated at **IC101**. Pb is adjusted in level with **VR105** and supplied to **IC104**. Pr is adjusted in level with **VR109** and supplied to **IC106**.

Y V is input from Encoder. **IC142** selects **Y V** or Y of external video input. After **VR104** adjusts the level, Y is converted to digital signal at **IC208**. DC level of clamp depends on **VR203**.

Sync. is separated from Y at **IC201**. PLL is composed of **IC205** of phase comparator, **X201** of 13.5MHz oscillator and **IC301**. This PLL generates the reference clock locked to input signal.

PB V is input from Encoder. **IC104** selects **PB V** or Pb of external video input. After **VR107** adjusts the timing and **VR108** adjusts the level, Pb is converted to digital signal at **IC207**. DC level of clamp depends on **VR204**.

PR V is input from Encoder. **IC106** selects **PR V** or Pr of external video input. After **VR111** adjusts the timing and **VR112** adjusts the level, Pr is converted to digital signal at **IC212**. DC level of clamp depends on **VR205**.

Y, Pb and **Pr** converted to 8bits of digital signal are supplied to **IC301**. Pb and Pr are mixed and supplied to Video Main P.C.Board as **YSI** and **CSI**. Each of those is 8bits of digital signal.

INH OUT is the pulse locked to input signal, which has the frequency of H. **INV OUT** is the pulse locked to input signal, which has the frequency of V. **INF OUT** is the pulse locked to input signal, which has the frequency of frame.

S DET output from **IC201** detection signal which is LOW when sync. is detected in external input.

VTR Syscon P.C.Board

This circuit is composed of CPU, Parallel I/O, Time Code and Character Generator.

Inputs from the operation panel are **ZEBRA, PLAY, STOP, FF, REW, EJECT, START, RET, SHUT, AWB** and **ABB SW**s. Those signals are supplied to **IC1** of CPU, via **IC201** of Parallel I/O.

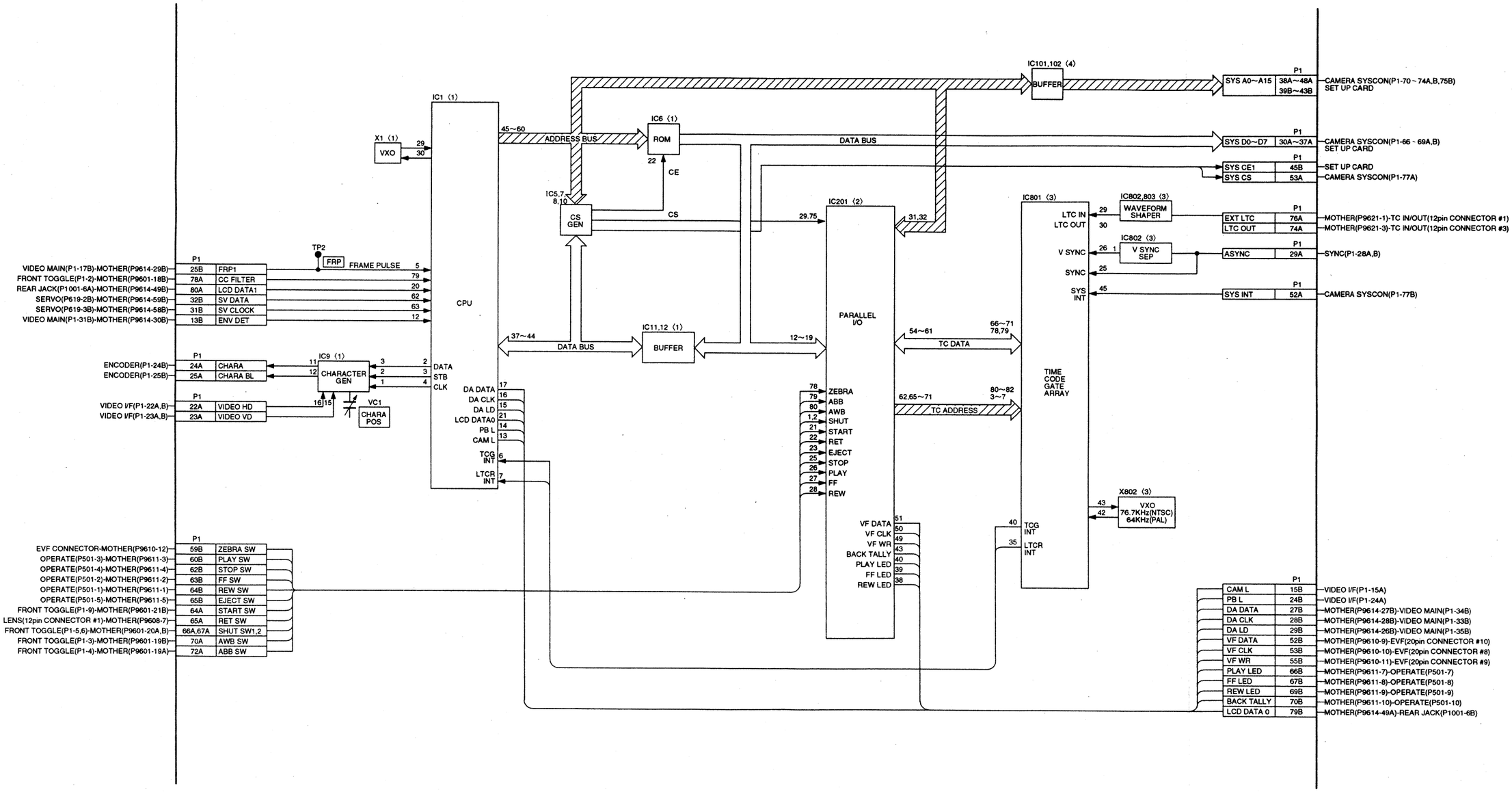
VTR Syscon and Camera Syscon communicate by **SYS A0～A15** and **SYS D0～D7**. **SYS A0～A15** are address lines. **SYS D0～D7** are data lines.

IC9 generates character. The character is supplied to Encoder P.C.Board.

IC801 is time code gate array which includes time code reader and generator. **29th** pin and **30th** pin are IN/OUT for external TC, which are supplied to 12 pins Multi Connector.

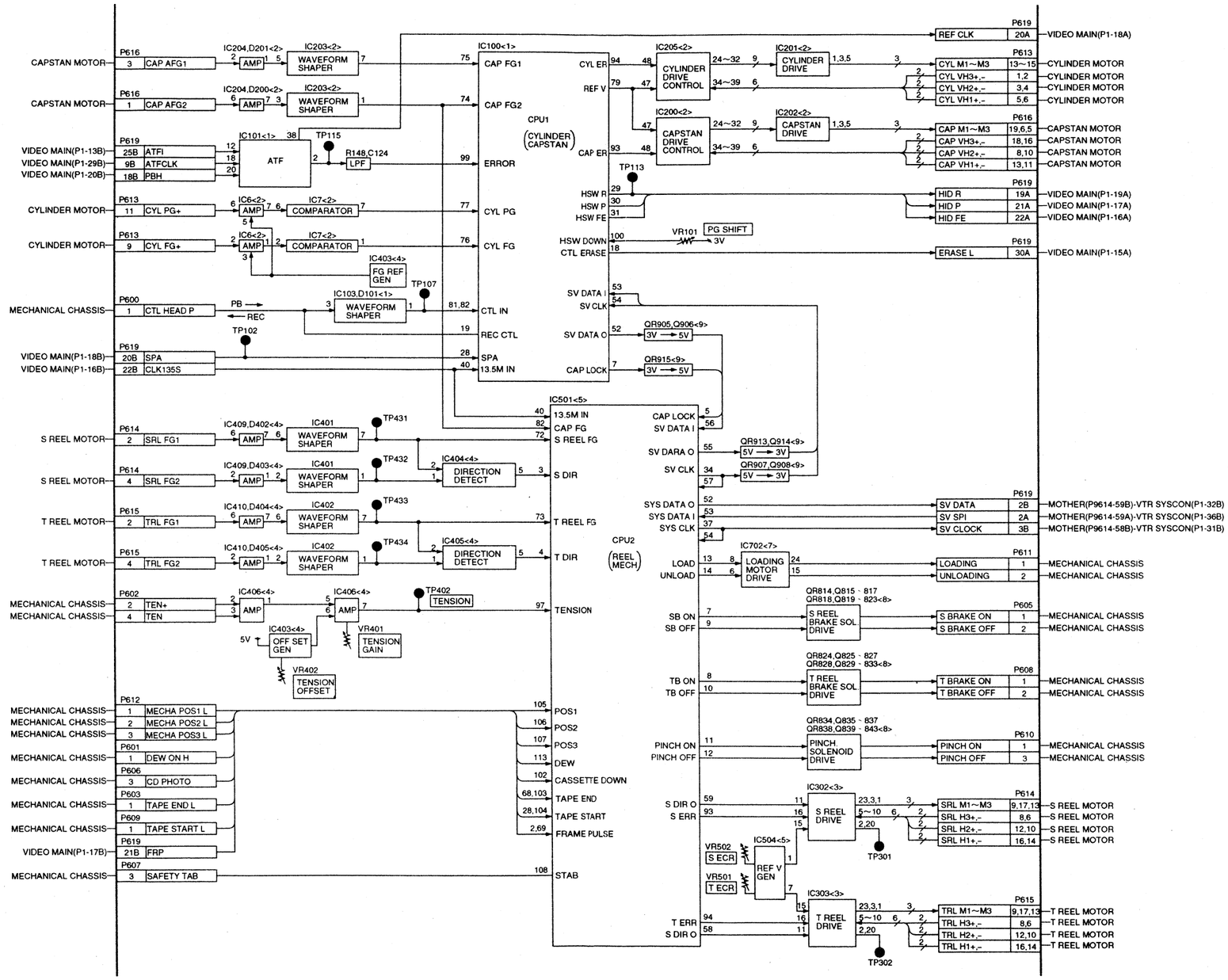
IC6 is Syscon ROM.

VTR SYSCON BLOCK DIAGRAM



1—21

SERVO BLOCK DIAGRAM



1—22

Servo P.C.Board

This circuit has two CPUs. **CPU1** controls cylinder and capstan. **CPU2** controls reel and mechanism.

CAP AFG1 and **CAP AFG2** are capstan FGs. Those are supplied to **IC100** of **CPU1**. **CAP M1～M3** drive the capstan. **CAP VH1～VH3** are fed back to **CPU1**.

CYL FG+ is cylinder FG. **CYL PG+** is cylinder PG. Those are supplied to **IC100** of **CPU1**. **CYL M1～M3** drive the cylinder. **CYL VH1～VH3** are fed back to **CPU1**.

HID R is R/P HSW. **HID P** is PB HSW. Played back CTL is input as **CTL HEAD P.** Recording CTL is also output as **CTL HEAD P**. **VR101** adjusts PG shifter which shifts HSW timing.

SRL FG1 and **SRL FG2** are S-reel FGs. Those are supplied to **IC501** of **CPU2**. **SRL M1～M3** drive the S-reel. **SRL H1～H3** are fed back to **CPU2**.

TRL FG1 and **TRL FG2** are T-reel FGs. Those are supplied to **IC501** of **CPU2**. **TRL M1～M3** drive the T-reel. **TRL H1～H3** are fed back to **CPU2**.

IC504 generates reference voltages which are comparated with error voltages, **S ERR** and **T ERR**. Reference voltages depend on **VR501** and **VR502**.

TEN+ and **TEN-** are input from tension sensor. **VR401** adjusts tension gain. **VR402** adjusts tension offset.

Abbreviations

ER, ERR	ERROR
DIR	DIRECTION
SV	SERVO
SB	S-REEL BRAKE
TB	T-REEL BRAKE
POS	POSITION

RF P.C.Board

(For recording) Input is **HSE**.(Top left) **EXT CW** is CW which is input from connector P2 when measuring C/N ratio. **IC1** selects **HSE** or **EXT CW**. **VR200** adjusts the duty of REC data at **IC208**. **Q208** and **Q209** are recording amplifiers for L ch. **REC CUR L** adjusts recording current(L ch). **REC FRE L** adjusts frequency characteristics(L ch). **Q202~Q205** switch mode REC or PB in L ch. **RP HEAD L P** and **N** are output to drum.

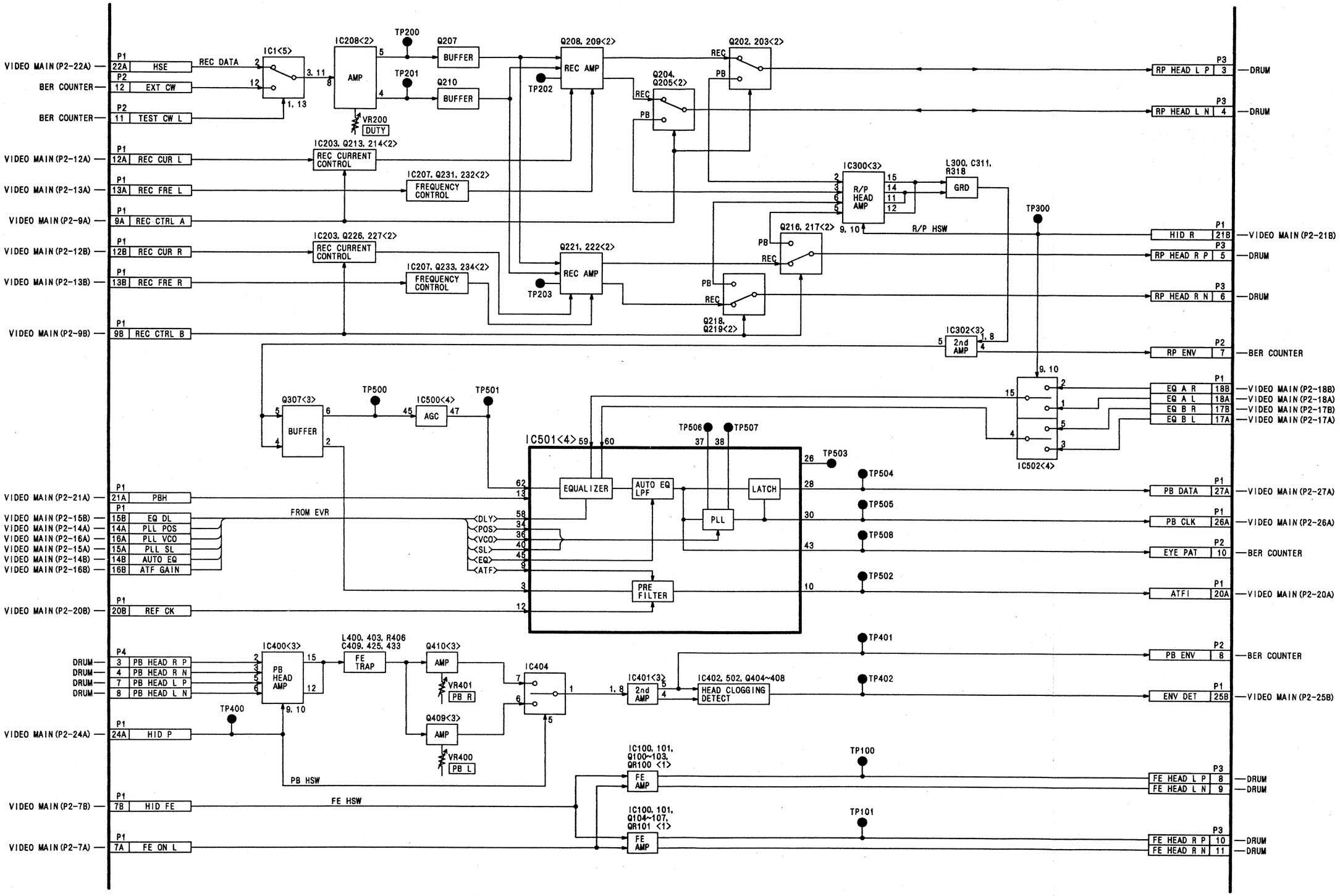
Q221 and **Q222** are recording amplifiers for R ch. **REC CUR R** adjusts recording current(R ch). **REC FRE R** adjusts frequency characteristics(R ch). **Q216~Q219** switch mode REC or PB in R ch. **RP HEAD R P** and **N** are output to drum.

(For playback) **RP HEAD L P** and **N** are input from drum for L ch and supplied to **IC300** of R/P Head Amp via **Q202~Q205**. **RP HEAD R P** and **N** are input from drum for R ch and supplied to **IC300** of R/P Head Amp via **Q226~Q219.** L ch and R ch are multiplexed at **IC300** by **HID R** which is R/P HSW. Both channels data are supplied to **IC501** and equalized by EVR data which are **EQ DL, PLL POS, PLL SL, AUTO EQ, EQ α R, EQ α L, EQ β R** and **EQ β L**. Outputs from **IC501** are **PB DATA** and **PB CLK**.

PB HEAD R P and **N** and **PB HEAD L P** and **N** are supplied to **IC400** which multiplexes R ch and L ch by **HID P** of PB HSW. Monitoring those signals detects head clogging. Information of head clogging is supplied to VIDEO MAIN P.C.Board as **ENV DET**. **VR400** and **VR401** adjusts detection levels. **FE TRAP** traps the frequency of A/C Head erase current.

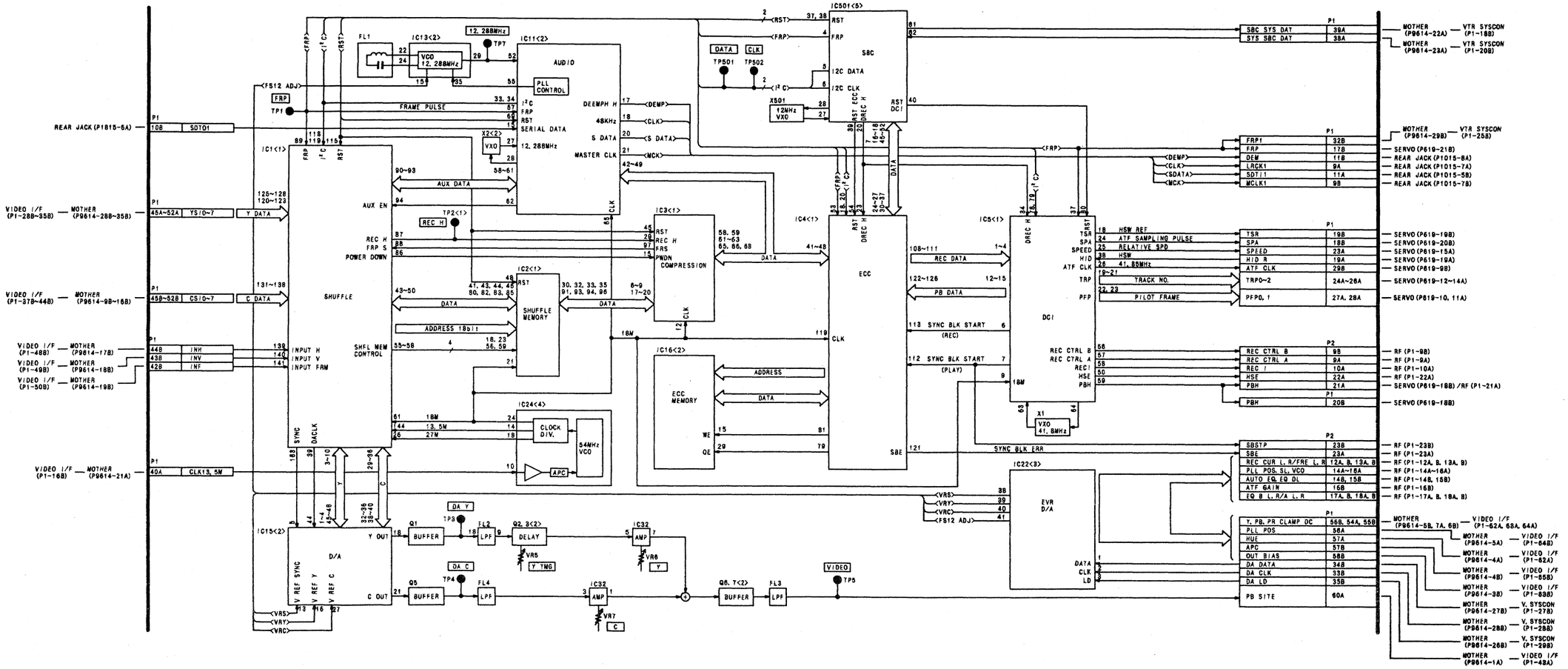
RP ENV, PB ENV and **EYE PAT** are available at BNCs of B.E.R.Counter.

RF BLOCK DIAGRAM



1—25

VIDEO MAIN BLOCK DIAGRAM



1—26

Video Main P.C.Board

This circuit processes shuffling, compression, ECC and 24-25 conversion for recording. In addition to this it makes a reverse process for playback.

(For recording) The Y to be recorded is input to **IC1**, SHUFFLE, as **YSI0~7**. The C to be recorded is also input to **IC1**, SHUFFLE, as **CSI0~7**. **IC2** is a shuffling memory. **IC24** supplies the clocks for **IC1**. Both signals of VIDEO are shuffled and supplied to **IC3** to be compressed.

Audio serial data, **SDTO1,** is supplied from AUDIO LCD P.C.Board to **IC11** via Rear Jack P.C.Board.

Audio signal is shuffled at **IC3**. Video data is compressed at **IC3**. Both are multiplexed and supplied to ECC of **IC4**. Video data is deshuffled at **IC4**. ECC codes are added to video and audio data, which are supplied to **IC5**.

IC5 is DCI which means the IC for digital signal processing. DCI makes two kinds of pilot signal for ATF. One has the frequency of 465kHz, the other has the frequency of 697.5kHz. DCI also makes 24-25 conversion.

HSE is the data to be recorded. **REC CTRL A** and **B** switch recording c

IC1, SHUFFLE, has another outputs of Y and C which are supplied to **IC15** of D/A converter to monitor playback picture. Y is adjusted in timing with **VR5** before mixing with C. Y level is adjusted with **VR6** at **IC32**. C level is adjusted with **VR7** at **IC32**. **PB SITE** is playback signal supplied to VIDEO I/F.

(For Playback) During playback the same circuit works the opposite process to recording.

(Others) **IC22** is D/A converter for EVR data. **IC501** is **SBC** which receives sub code data from VTR Syscon P.C.Board and adds it to video data.

Audio LCD P.C.Board

This circuit has three kinds of audio inputs.

CH1 IN H and **CH1 IN C** are supplied to **RY101** where attenuater ON/OFF is switched. **CH2 IN H** and **CH2 IN C** are supplied to **RY201** where attenuater ON/OFF is switched. **F MIC IN H** and **F MIC IN C** are inputs from front microphone. When phantom microphone is used, 48V is supplied based on **SW 12V**. All of those are supplied to **IC1** of MIC AMP where gains are controlled by **IC603**, Audio CPU.

CH1 is output from the **24th** pin of **IC1**. **SW701** switches balance or unbalance output for 26pin connector. **IC15** of HPF cuts the wind noise. **IC4** switches the HPF ON/OFF. **VR101** coarsely adjusts the level. **FRONT VR** which comes from the VR in front of camera recorder also adjusts CH1 recording level. **IC105** switches the mode. **VR102** adjusts recording level. **IC6** and **Q4** of TEST SG generate 1kHz of tone signal. The level of test tone is adjusted with **VR2**. **IC105** switches test tone or input audio. The signal to be recorded is A/D converted at **IC8** and supplied to Video Main P.C.Board via Rear Jack P.C.Board as **SDTO1**.

CH2 is output from the **13th** pin of **IC1**. **IC15** of HPF cuts the wind noise. **IC4** switches the HPF ON/OFF. **VR201** coarsely adjusts the level. **IC205** switches the mode. **VR202** adjusts recording level. **IC205** switches test tone or input audio.

The audio signal for output is input as **SDTI1** from Video Main P.C.Board via Rear Jack P.C.Board. It is D/A converted at **IC8** and supplied to MIX AMP and MONITOR SELECT. **IC6** and **IC10** of MIX AMP mixes CH1 and CH2. **IC11** selects CH1, CH2 or MIX as monitor outputs L ch and R ch. Selected signal or cue audio is selected at **IC12**. Monitor outputs are supplied as **MON VR IN L** and **R** to ALARM/MONITOR P.C.Board. They return as **MON VR OUT L** and **R** with alarm, **ALARM VR OUT**. **HP OUT L** and **R** are for headphone. **SP OUT** is for speaker.

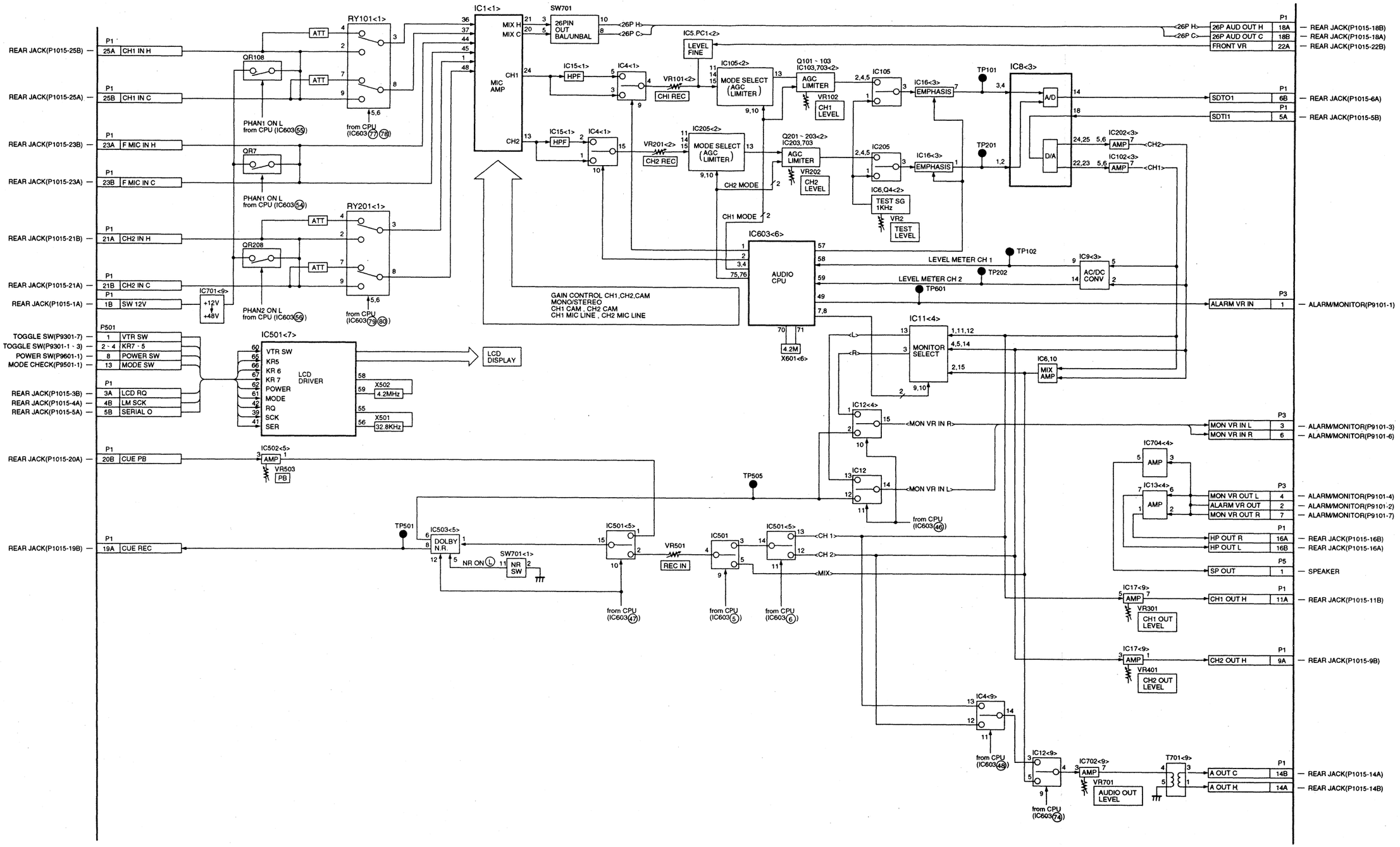
IC17 adjusts CH1 OUT level and CH2 OUT level with **VR301** and **VR401**. Those outputs, **CH1 OUT H** and **CH2 OUT H**, are supplied to 12pin multi connector.

IC501 selects recording signal for CUE audio. **VR501** adjusts recording level in CUE audio. **VR503** adjusts playback level in CUE audio.

A OUT H and **C** are supplied to Rear Jack P.C.Board for AUDIO OUT. **VR701** adjusts the level.

IC501 drives LCD.

AUDIO LCD BLOCK DIAGRAM



1—29

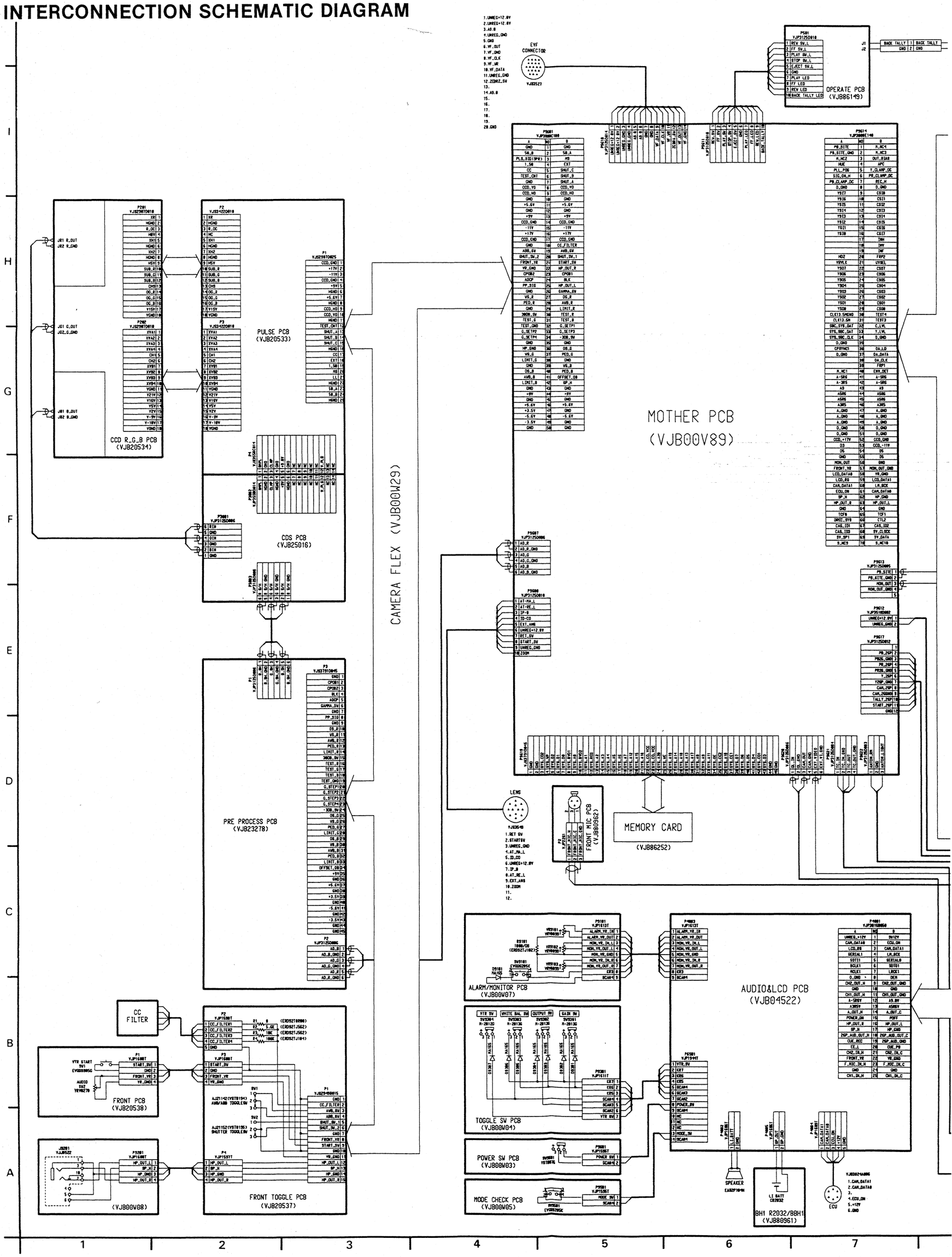
SECTION 2

SCHEMATIC DIAGRAMS

CONTENTS

Schematic Diagrams

INTERCONNECTION SCHEMATIC DIAGRAM



SV1 VST0131 — D1 TLR411G — BACK TALLY PCB (VJB80858)

from MECHANISM

SERVO PCB (VJB02437)

RF PCB (VJB03B95)

POWER PCB (VJB01643)

VTR FLEX (VJB80980)

REAR JACK PCB (VJB01642)

DC INPUT PCB (VJB00X87) — (VJB00W08)

BNC PCB (VJB80981)

TC IN/OUT AUDIO OUT VJ035-8

CAPSTAN MOTOR

CYLINDER MOTOR

S_REEL MOTOR

T_REEL MOTOR

26P CONNECTOR VJP1957

EXT VIDEO IN VJS14-8

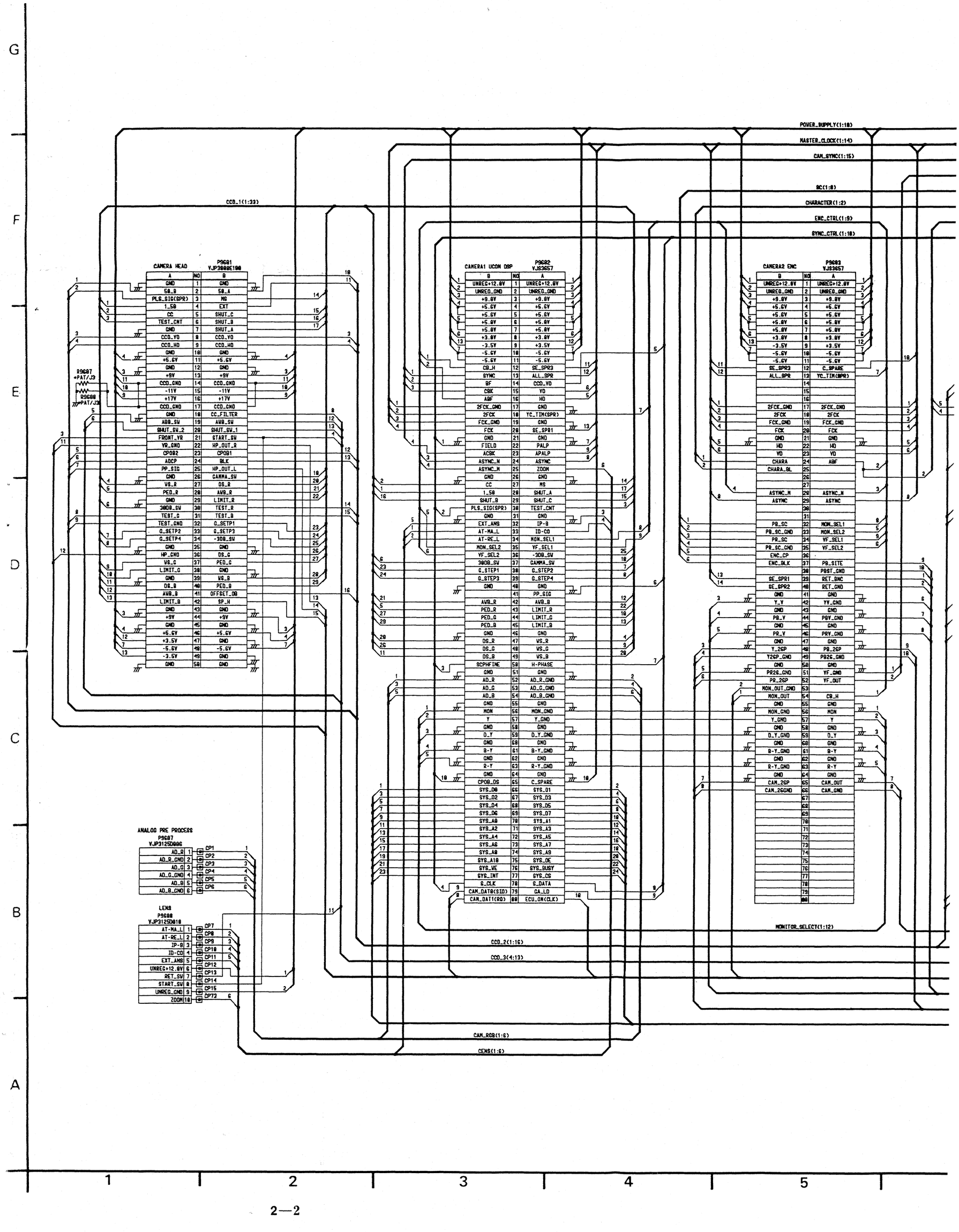
1.COMPOSITE VIDEO
2.COMPOSITE GND
3.Y_GND
4.Y
5.PR
6.PR_GND
7.PB
8.PB_GND
9.CAM_MIC(H)
10.CAM_MIC(C)
11.CAM_MIC(G)
12.VTR START/STOP
15.REC TALLY
8 GND

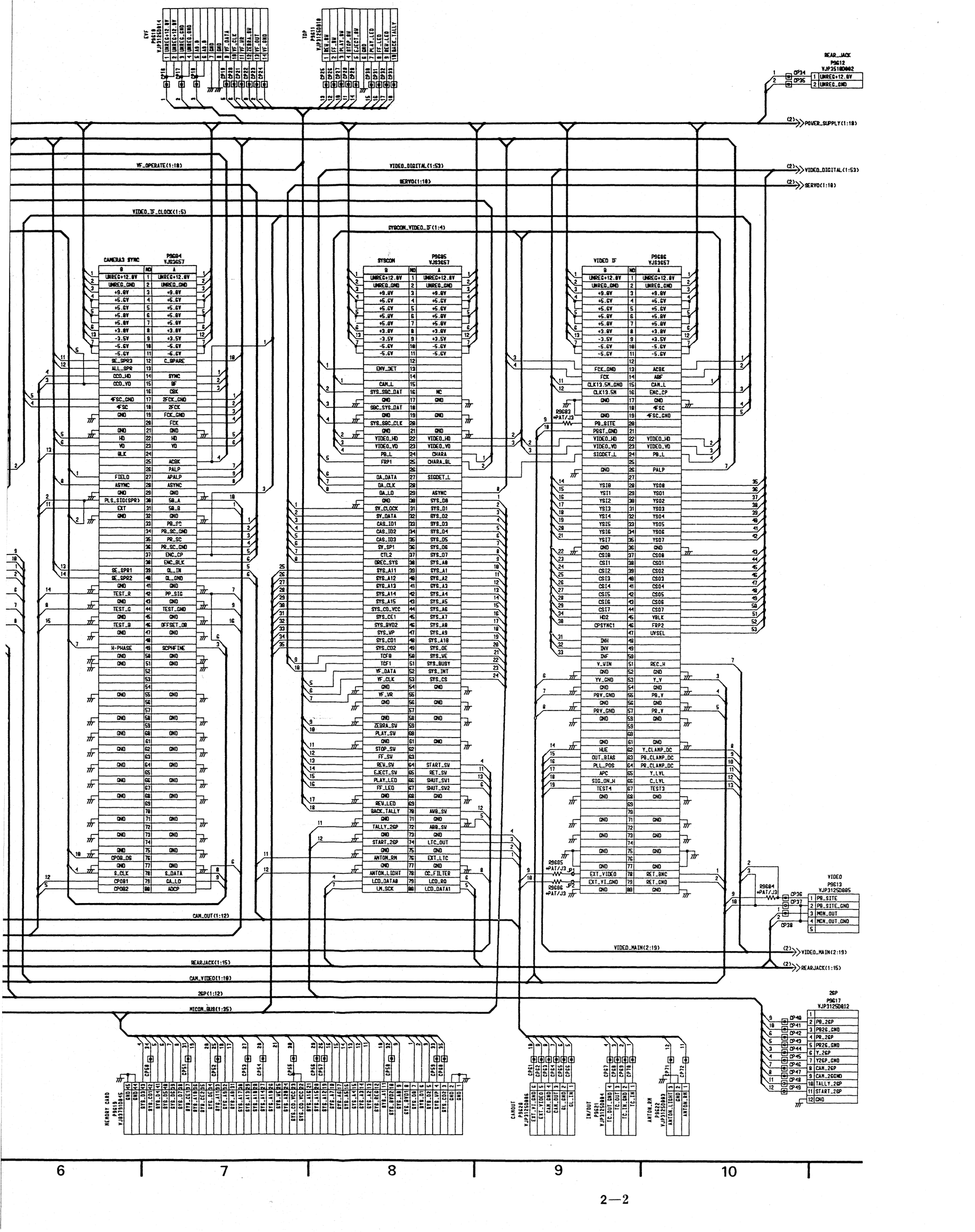
1.TC IN
2.TC IN GND
3.TC OUT
4.TC OUT GND
5.CH1_OUT
6.
7.CH1_OUT_GND
8.CH2_OUT
9.
10.CH2_OUT_GND
11.
12.

7 8 9 10 11 12 13 14

REVERSE SIDE

MOTHER SCHEMATIC DIAGRAM




EVF
P9618
VJP3125D014
TOP
P9611
VJP3125D010
REAR_JACK
P9612
VJP3510D002
POWER_SUPPLY(1:18)
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VIDEO_IF_CLOCK(1:5)
SYSCON_VIDEO_IF(1:4)
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P9685
VJS3657
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REARJACK(1:15)
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MICOM_BUS(1:35)
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VJP3125D005
2SP
P9617
VJP3125D012
MEMORY CARD
P9619
VJP3751D045
CAMOUT
P9624
VJP3125D006
IN/OUT
P9623
VJP3125D004
ANTON_RM
P9622
VJP3125D003
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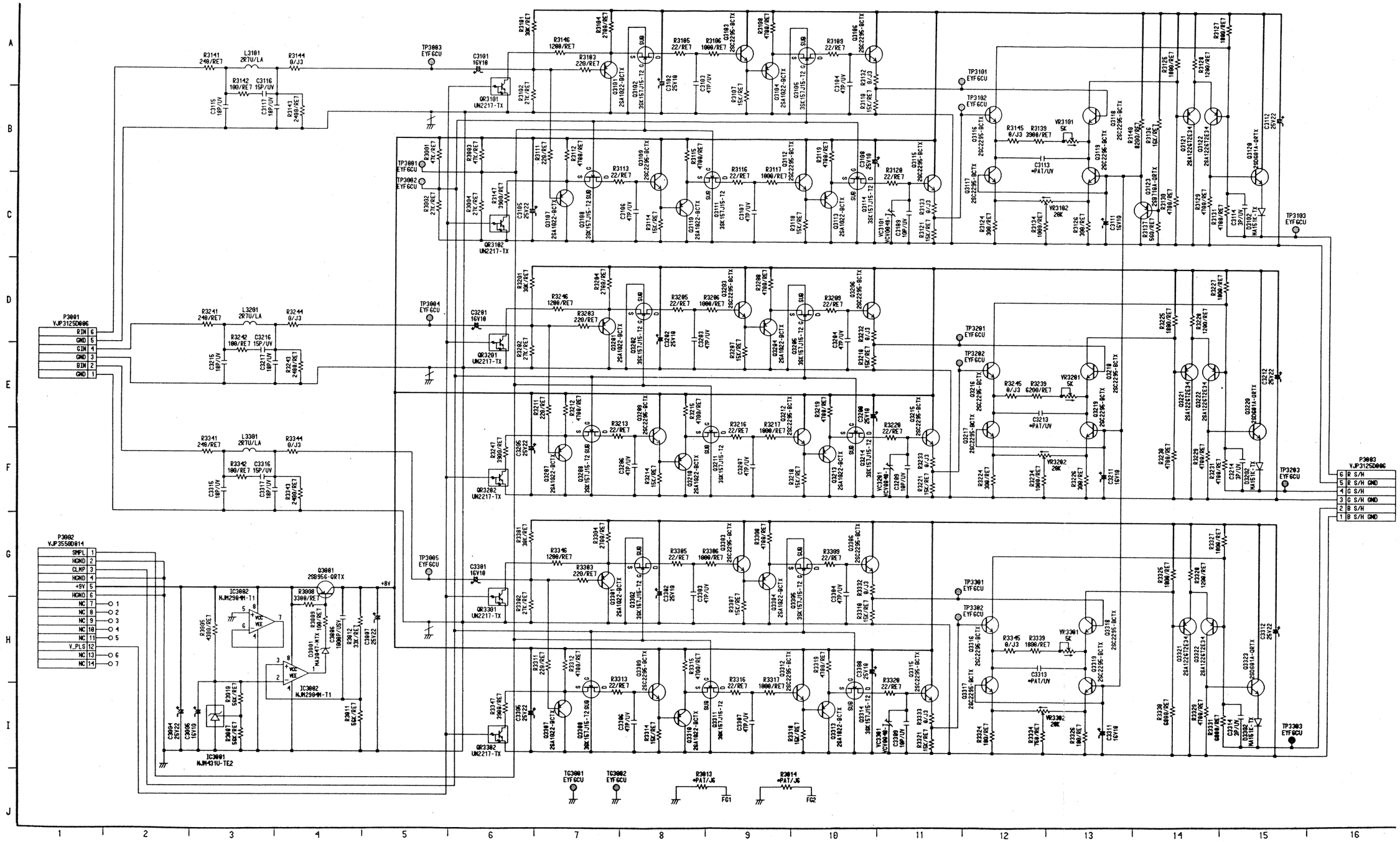
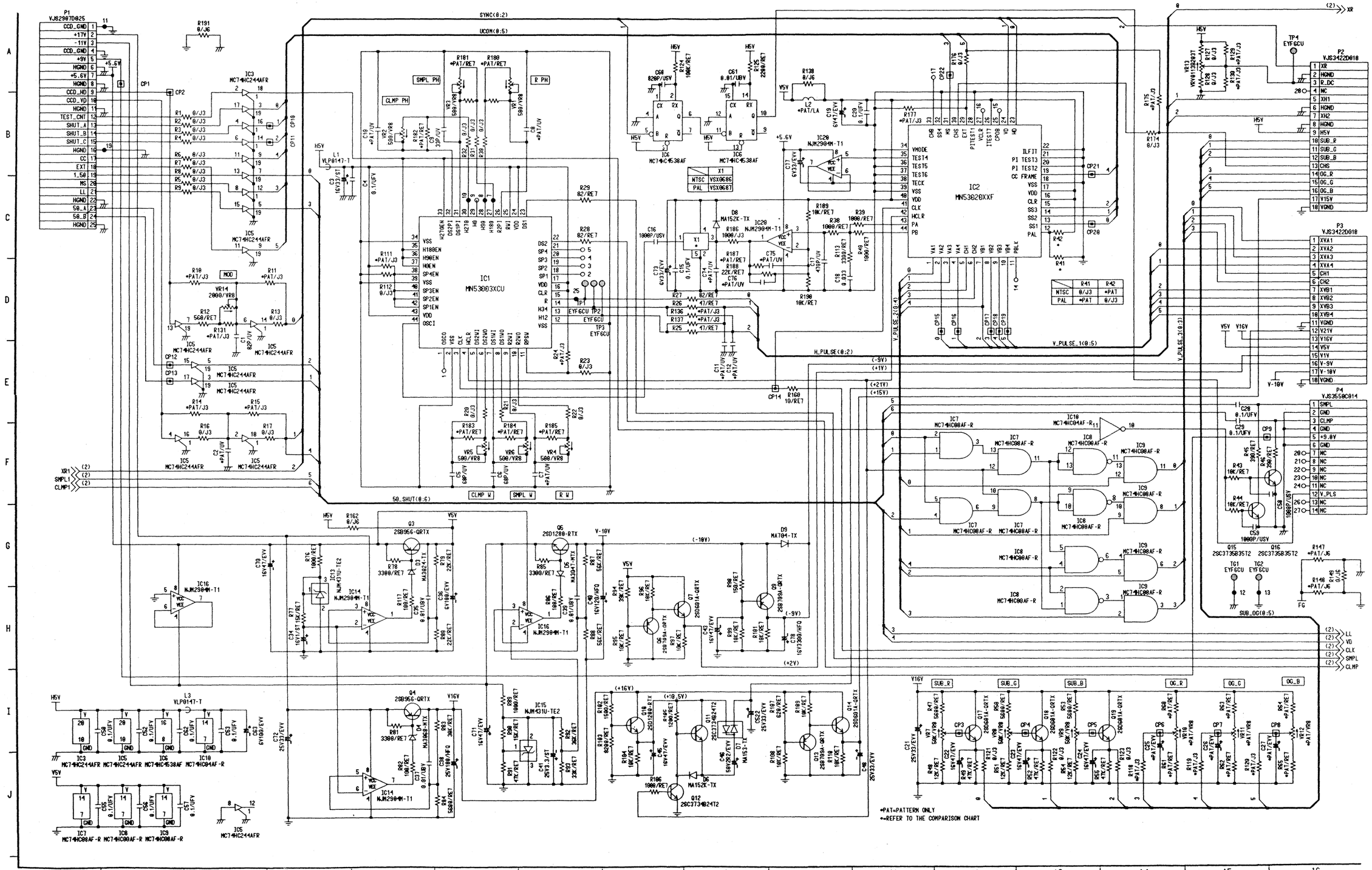
CDS SCHEMATIC DIAGRAM



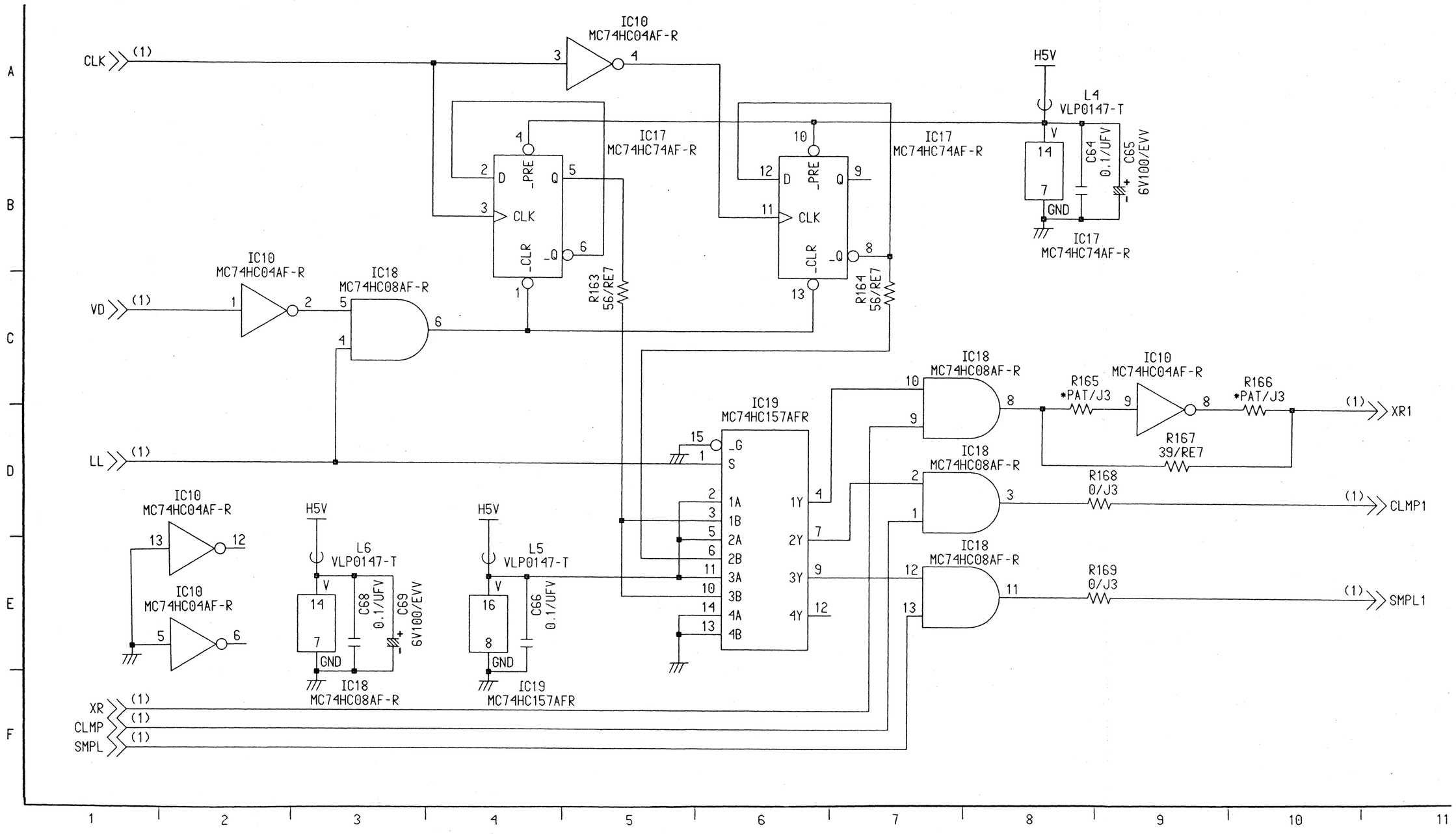
2—3

PULSE (1/4) SCHEMATIC DIAGRAM



REVERSE SIDE

PULSE (2/4) SCHEMATIC DIAGRAM



2—5

PULSE (3/4) COMPARISON CHART 1 BETWEEN MODELS

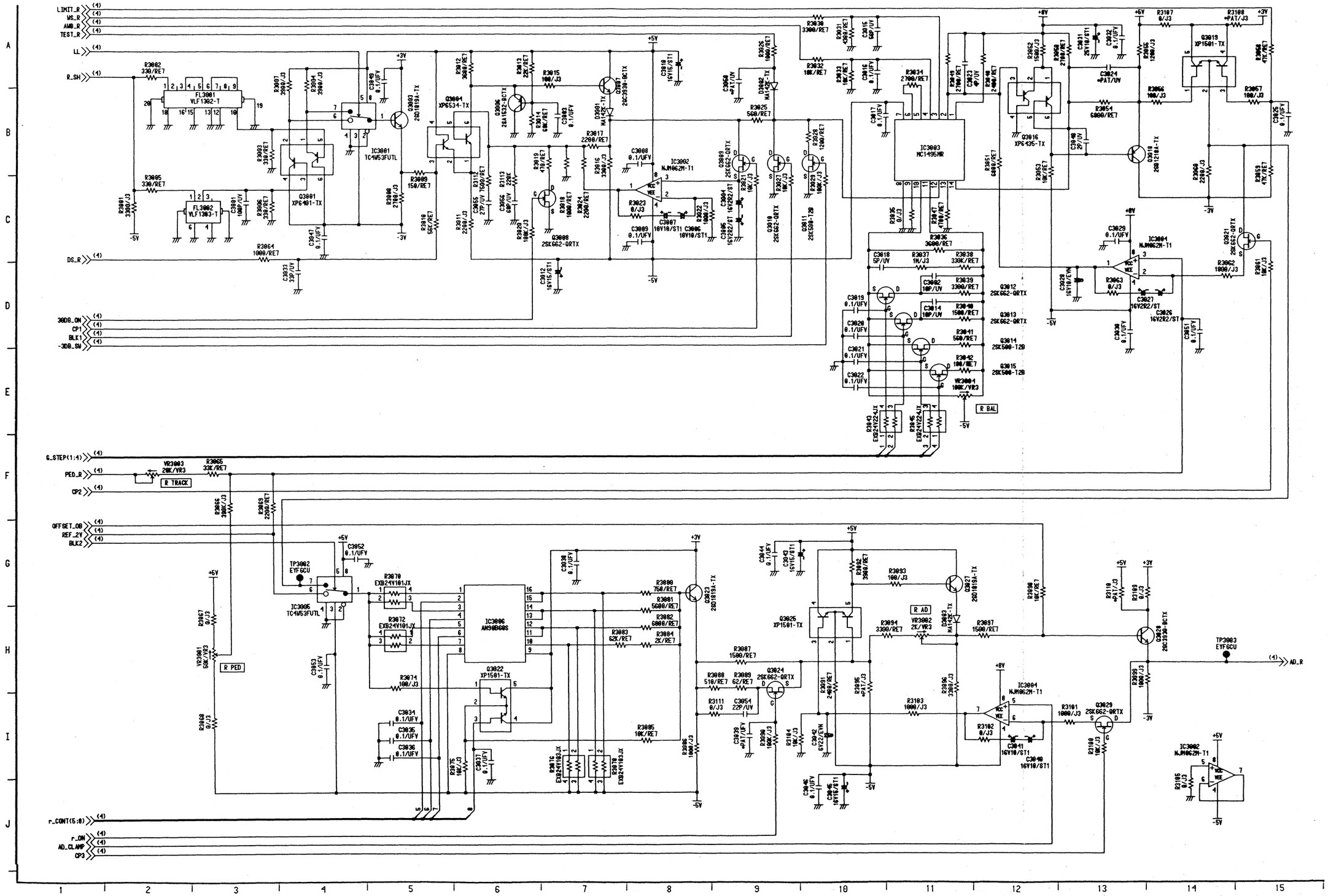
REF	NTSC	PAL	ON
C10	*PAT/UV	*PAT/UV	56P/UV
C11	*PAT/UV	*PAT/UV	56P/UV
C12	*PAT/UV	*PAT/UV	56P/UV
C2	*PAT/UV	*PAT/UV	56P/UV
C25	*PAT/EVV	*PAT/EVV	16V10/EVV
C26	*PAT/EVV	*PAT/EVV	16V10/EVV
C27	*PAT/EVV	*PAT/EVV	16V10/EVV
C7	*PAT/UV	*PAT/UV	33P/UV
C74	*PAT/UV	*PAT/UV	33P/UV
C75	*PAT/UV	*PAT/UV	33P/UV
C76	*PAT/UV	*PAT/UV	33P/UV
C8	*PAT/UV	*PAT/UV	33P/UV
L2	*PAT/LA	*PAT/LA	33U/LA
R10	*PAT/J3	*PAT/J3	0/J3
R11	*PAT/J3	*PAT/J3	0/J3
R111	*PAT/J3	*PAT/J3	0/J3
R118	*PAT/J3	*PAT/J3	0/J3
R119	*PAT/J3	*PAT/J3	0/J3
R120	*PAT/J3	*PAT/J3	0/J3
R129	*PAT/RE7	*PAT/RE7	22K/RE7
R130	*PAT/RE7	*PAT/RE7	22K/RE7
R131	*PAT/J3	*PAT/J3	0/J3
R136	*PAT/J3	*PAT/J3	0/J3
R137	*PAT/J3	*PAT/J3	0/J3
R14	*PAT/J3	*PAT/J3	0/J3
R147	*PAT/J6	*PAT/J6	0/J6
R148	*PAT/J6	*PAT/J6	0/J6
R15	*PAT/J3	*PAT/J3	0/J3
R165	*PAT/J3	*PAT/J3	0/J3
R166	*PAT/J3	*PAT/J3	0/J3
R175	*PAT/J3	*PAT/J3	0/J3
R177	*PAT/J3	*PAT/J3	0/J3
R180	*PAT/RE7	*PAT/RE7	510/RE7
R181	*PAT/RE7	*PAT/RE7	270/RE7
R182	*PAT/RE7	*PAT/RE7	270/RE7
R183	*PAT/RE7	*PAT/RE7	270/RE7
R184	*PAT/RE7	*PAT/RE7	270/RE7
R185	*PAT/RE7	*PAT/RE7	510/RE7
R187	*PAT/RE7	*PAT/RE7	22K/RE7
R24	*PAT/J3	*PAT/J3	0/J3
R41	0/J3	*PAT/J3	0/J3
R42	*PAT/J3	0/J3	0/J3
R60	*PAT/RE7	*PAT/RE7	15K/RE7

REVERSE SIDE
PULSE 2/4

PULSE (4/4) COMPARISON CHART 2 BETWEEN MODELS

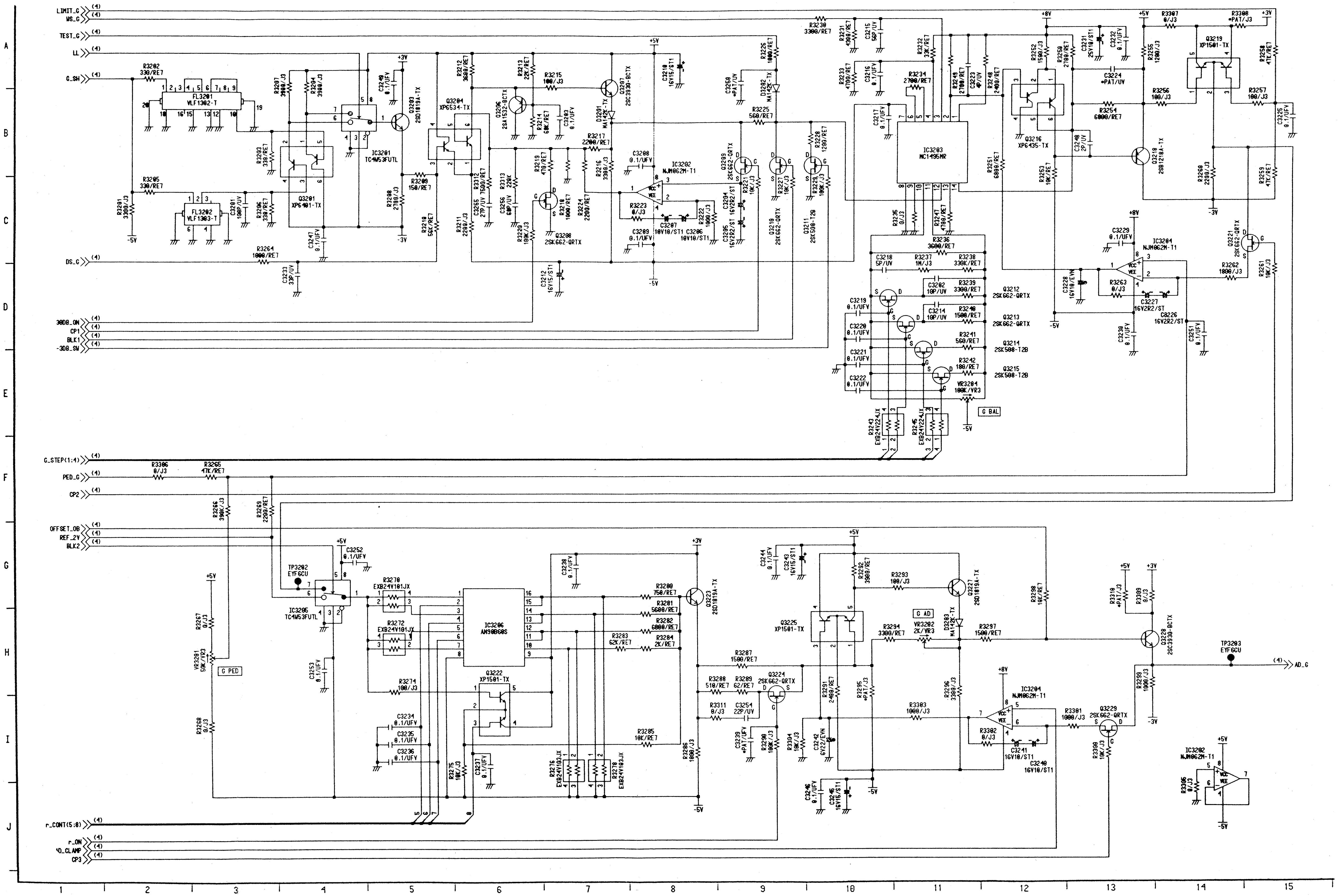
REF	NTSC	PAL	ON
R61	*PAT/RE7	*PAT/RE7	3300/RE7
R62	*PAT/RE7	*PAT/RE7	3300/RE7
R63	*PAT/RE7	*PAT/RE7	15K/RE7
R64	*PAT/RE7	*PAT/RE7	15K/RE7
R65	*PAT/RE7	*PAT/RE7	3300/RE7
VR10	*PAT/VR8	*PAT/VR8	20K/VR8
VR11	*PAT/VR8	*PAT/VR8	20K/VR8
VR12	*PAT/VR8	*PAT/VR8	20K/VR8
X1	VSX0686	VSX0687	VSX0686

PRE PROCESS (1/4) SCHEMATIC DIAGRAM



2—7

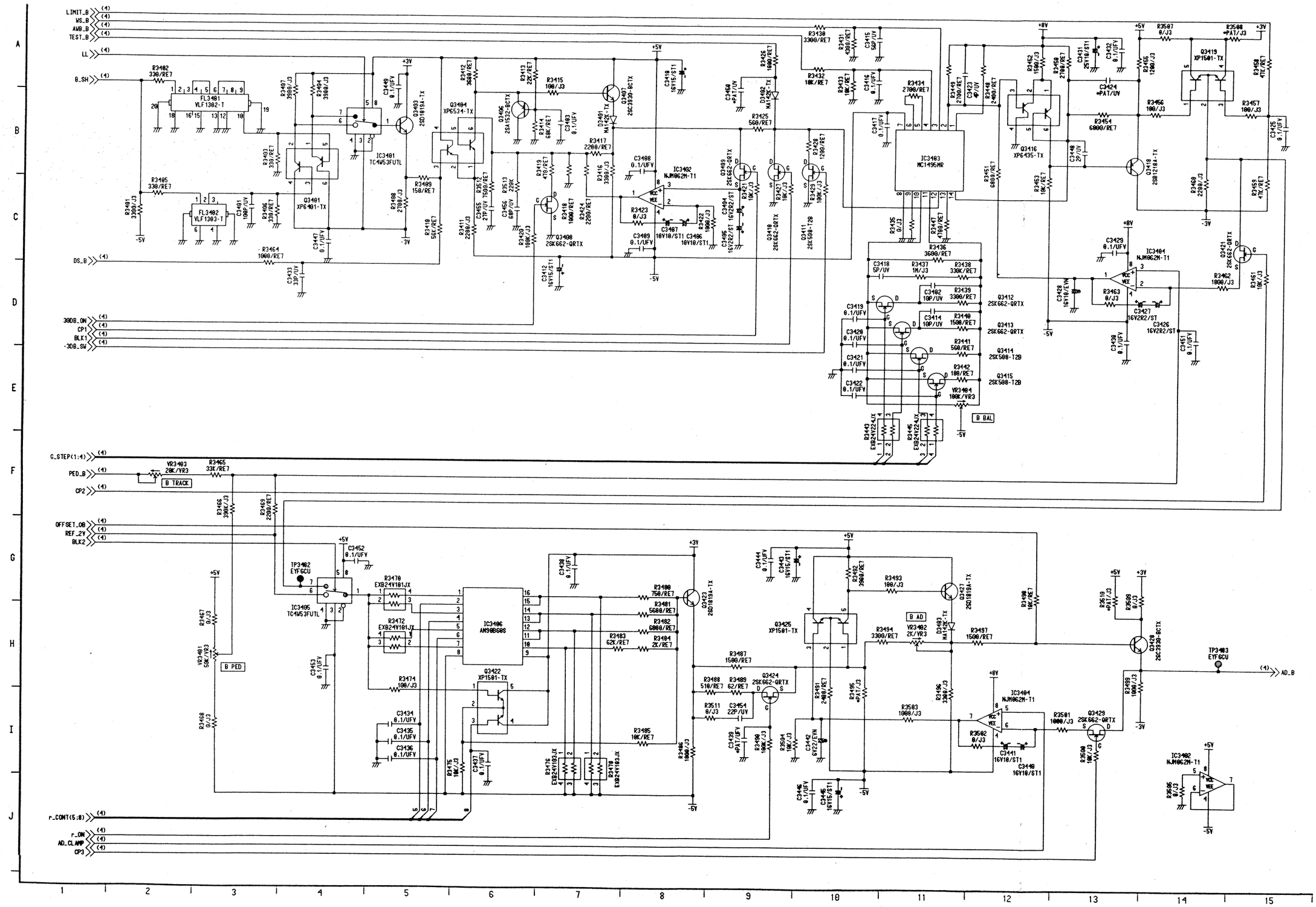
PRE PROCESS (2/4) SCHEMATIC DIAGRAM



REVERSE SIDE

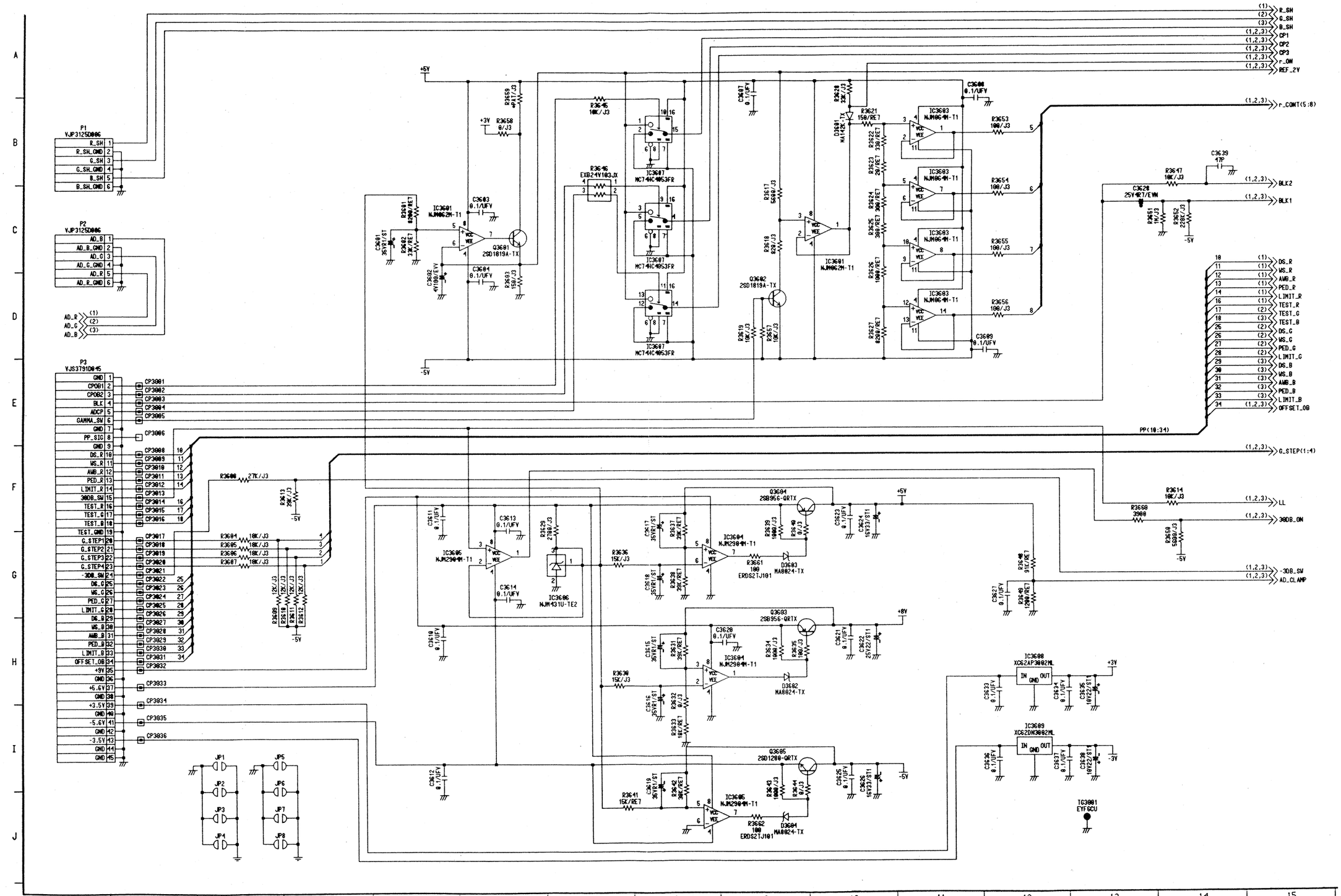
PRE PROCESS 1/4

PRE PROCESS (3/4) SCHEMATIC DIAGRAM



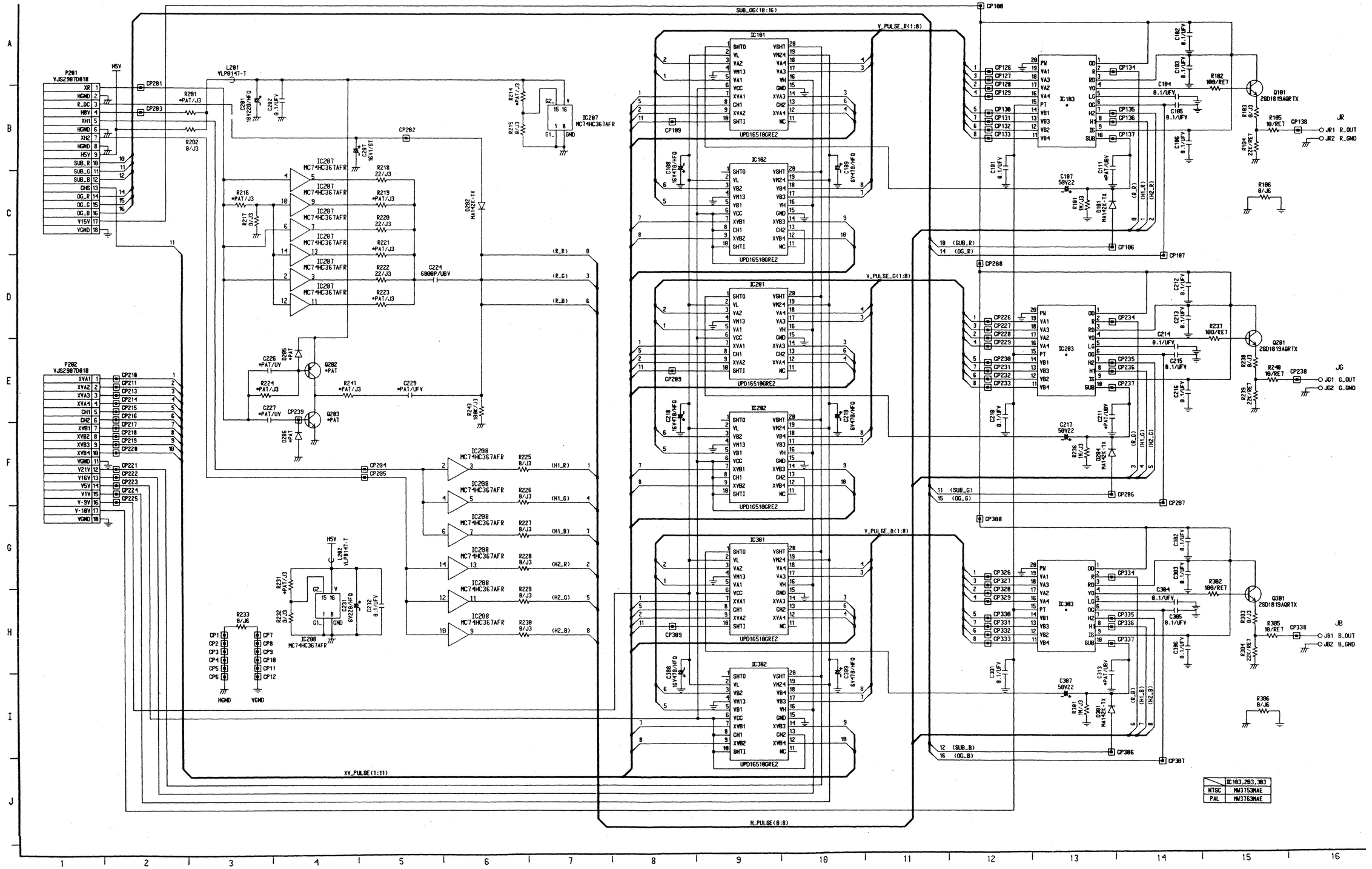
2—9

PRE PROCESS (4/4) SCHEMATIC DIAGRAM



REVERSE SIDE

CCD (1/2) SCHEMATIC DIAGRAM



2—11

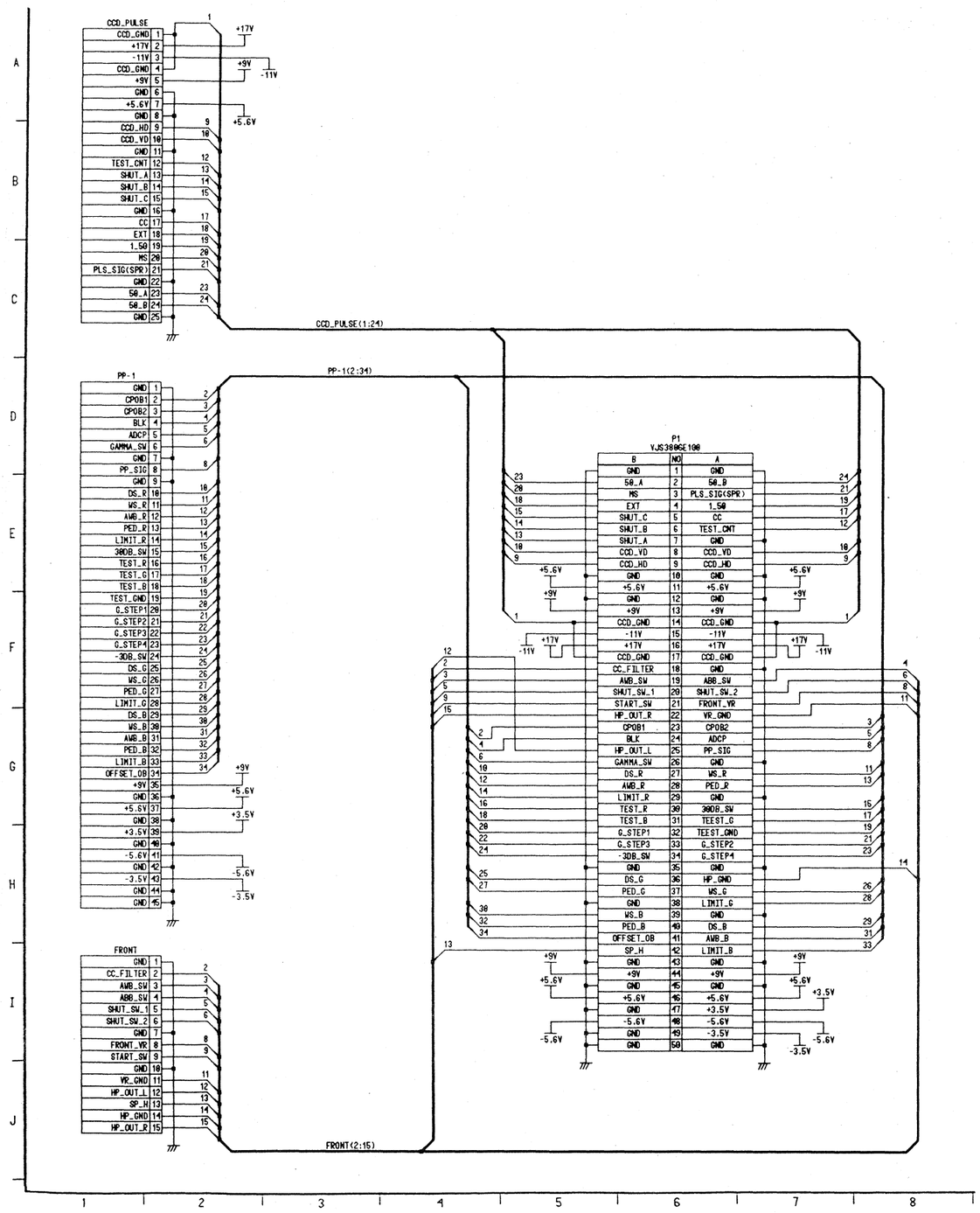
CCD (2/2) COMPARISON CHART BETWEEN MODELS

REF	NTSC	PAL	ON
C111	*PAT/UBV	*PAT/UBV	6800P/UBV
C211	*PAT/UBV	*PAT/UBV	6800P/UBV
C226	*PAT/UV	*PAT/UV	220P/UV
C227	*PAT/UV	*PAT/UV	180P/UV
C229	*PAT/UFV	*PAT/UFV	0. 1/UFV
C313	*PAT/UBV	*PAT/UBV	6800P/UBV
D205	*PAT	*PAT	MA141K-TX
D206	*PAT	*PAT	MA141K-TX
IC103	MW3753MAE	MW3763MAE	MW3753MAE
IC203	MW3753MAE	MW3763MAE	MW3753MAE
IC303	MW3753MAE	MW3763MAE	MW3753MAE
Q202	*PAT	*PAT	2SB1218AQRTX
Q203	*PAT	*PAT	2SD1819AQRTX
R201	*PAT/J3	*PAT/J3	0/J3
R214	*PAT/J3	*PAT/J3	0/J3
R216	*PAT/J3	*PAT/J3	0/J3
R219	*PAT/J3	*PAT/J3	22/J3
R221	*PAT/J3	*PAT/J3	22/J3
R223	*PAT/J3	*PAT/J3	22/J3
R224	*PAT/J3	*PAT/J3	1M/J3
R231	*PAT/J3	*PAT/J3	0/J3
R241	*PAT/J3	*PAT/J3	22/J3

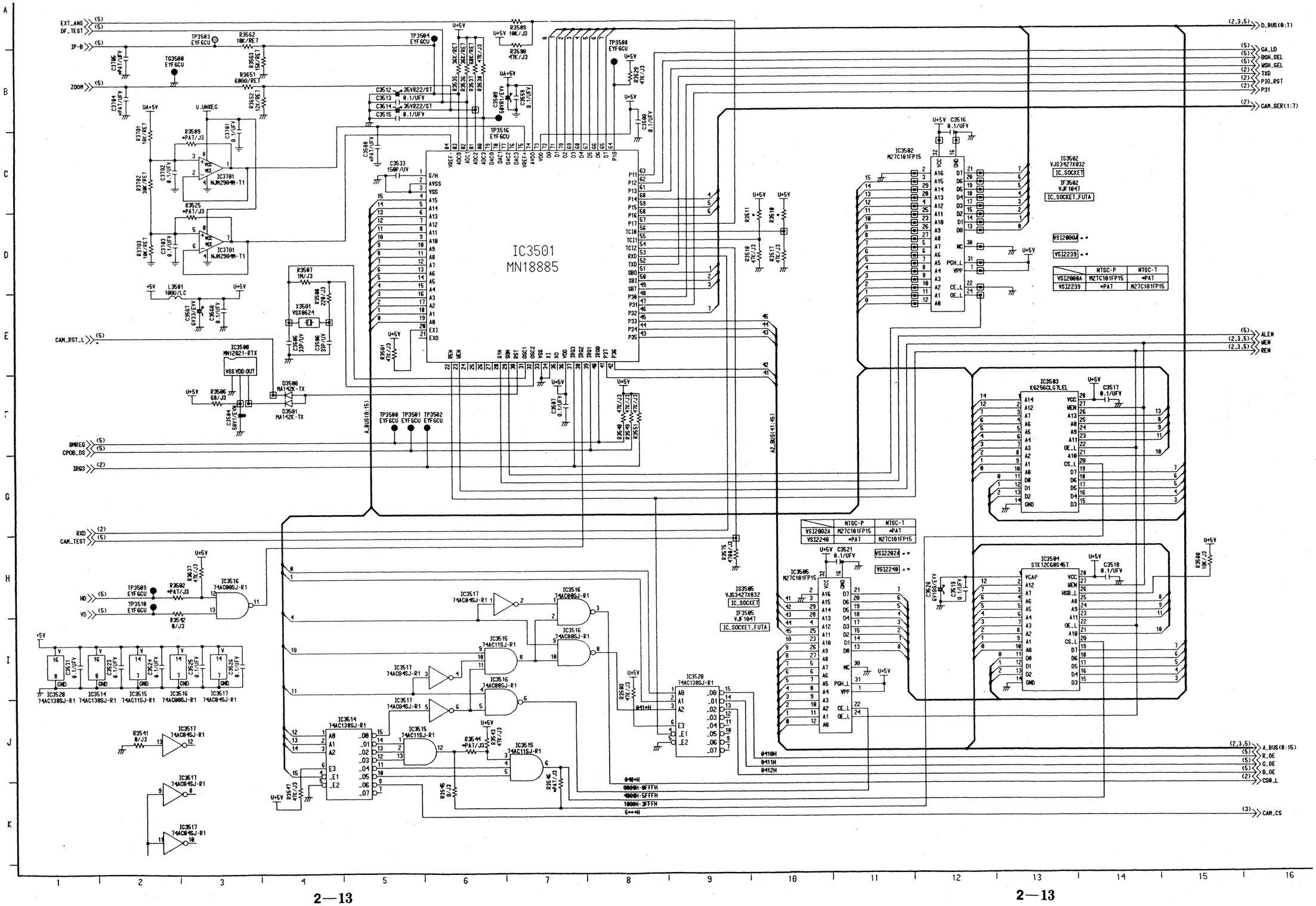
REVERSE SIDE

CCD 1/2

CAMERA FLEX SCHEMATIC DIAGRAM

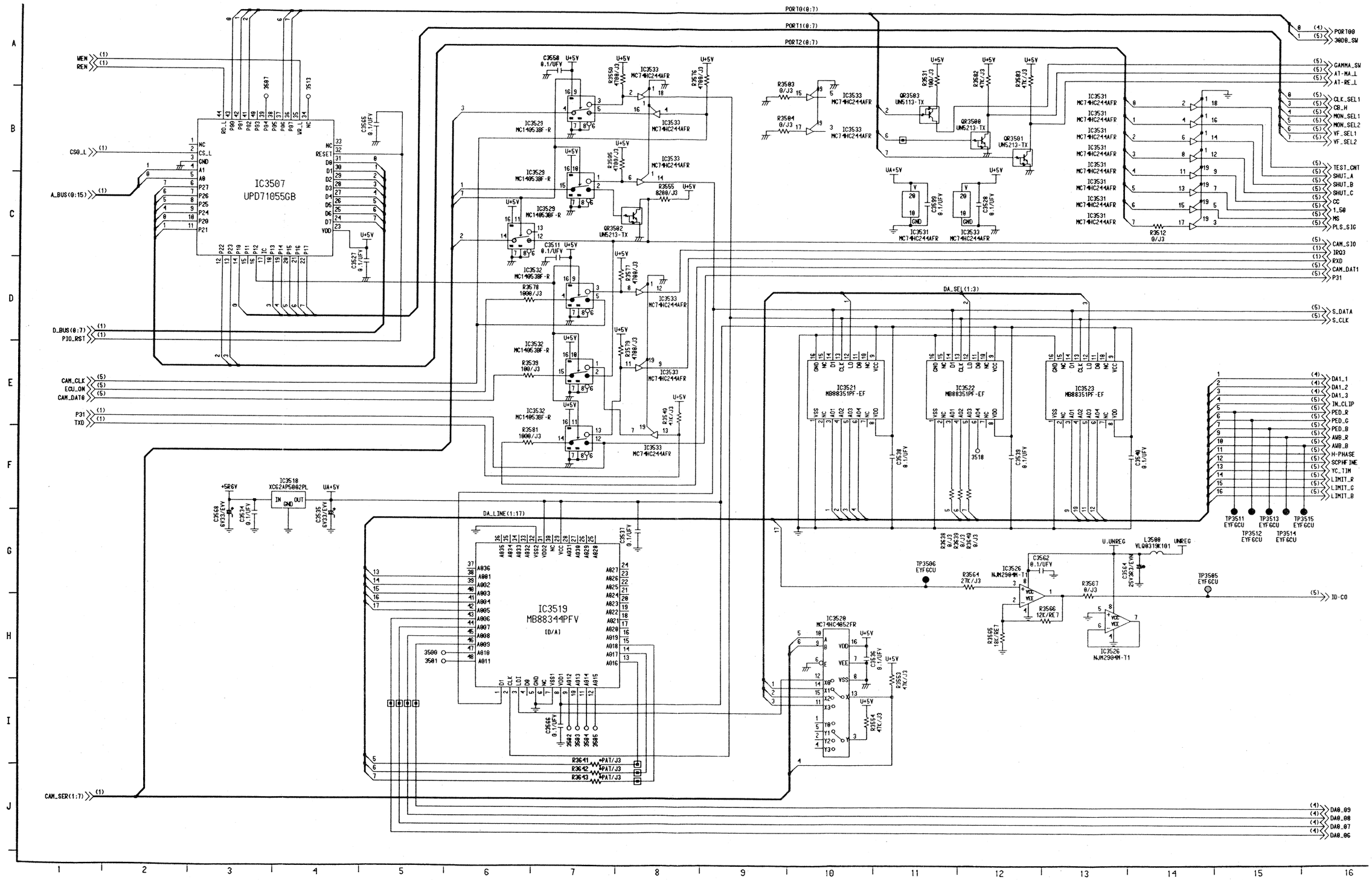


CAMERA SYSCON (1/5) SCHEMATIC DIAGRAM



2—13

CAMERA SYSCON (2/5) SCHEMATIC DIAGRAM

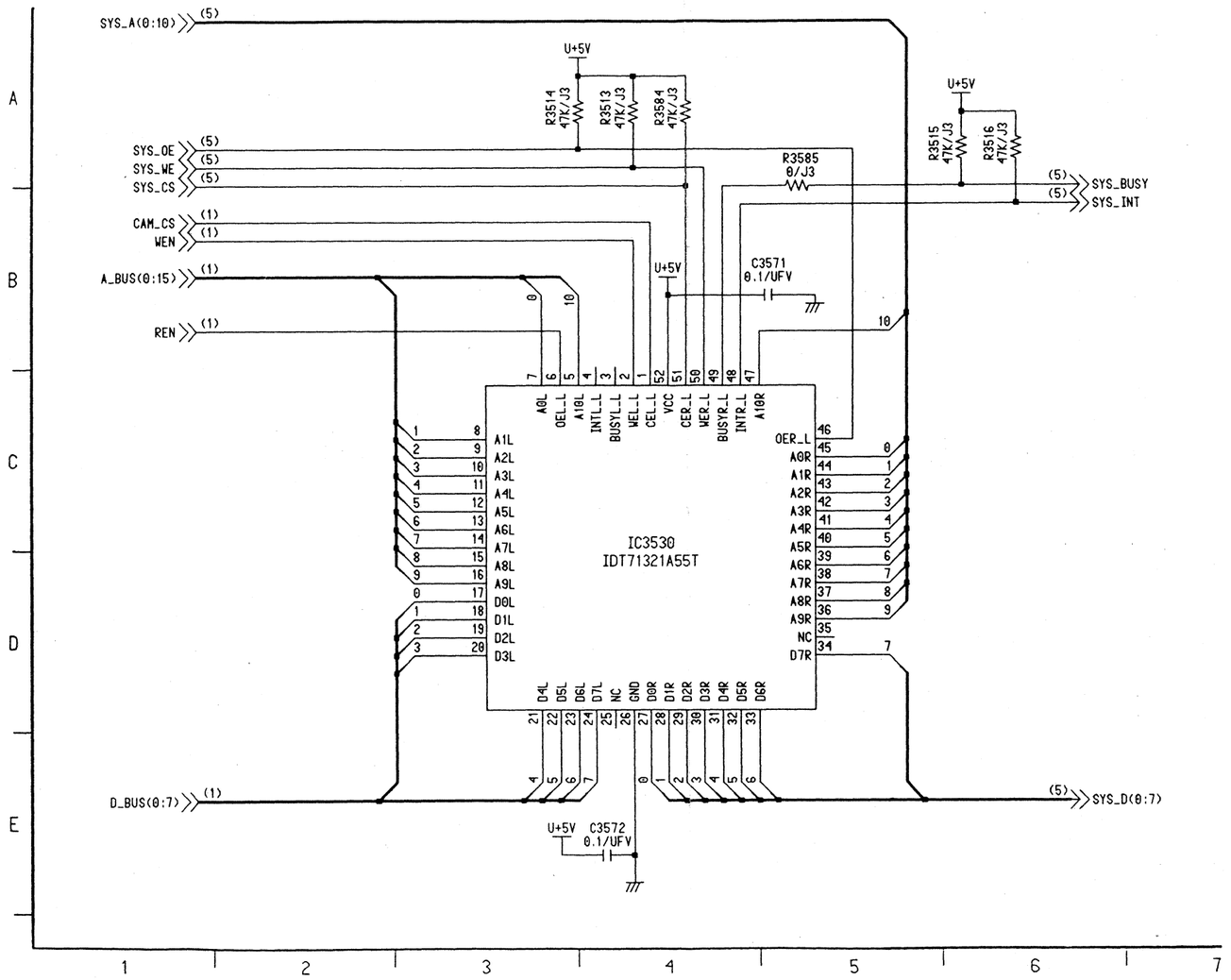


CAMERA SYSCON 1/5

2—14

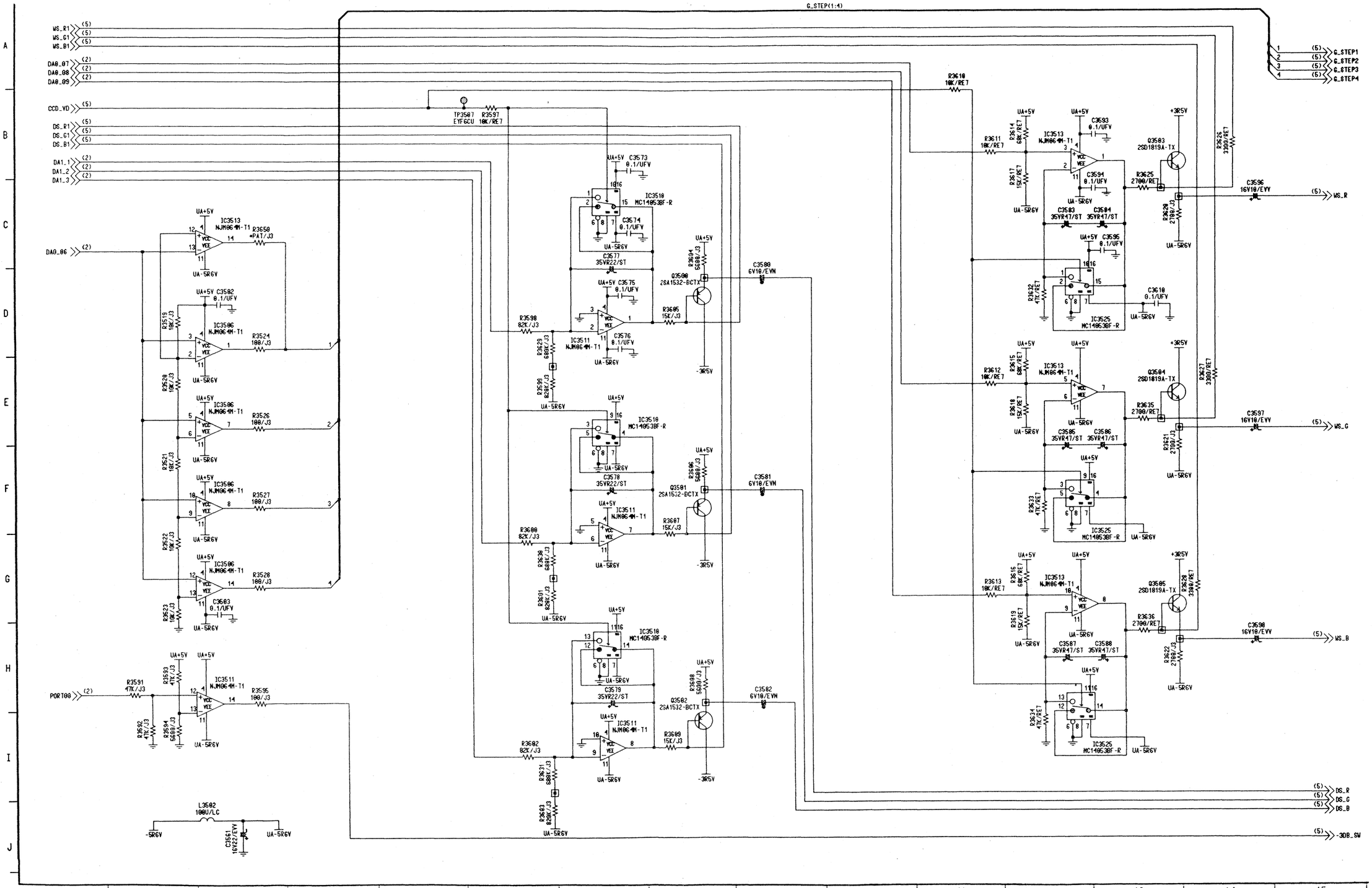
REF	VAL	PAL	NTSC-P	NTSC-T	ON
C3508	*PAT/UFV	*PAT/UFV	*PAT/UFV	*PAT/UFV	0.1/UFV
C3704	*PAT/UFV	*PAT/UFV	*PAT/UFV	*PAT/UFV	0.1/UFV
C3705	*PAT/UFV	*PAT/UFV	*PAT/UFV	*PAT/UFV	0.1/UFV
R3502	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3509	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3511	*PAT/J3	10K/J3	*PAT/J3	*PAT/J3	10K/J3
R3518	*PAT/J3	*PAT/J3	*PAT/J3	10K/J3	10K/J3
R3525	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3544	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3546	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3641	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3642	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3643	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3650	*PAT/J3	*PAT/J3	*PAT/J3	*PAT/J3	0/J3

CAMERA SYSCON (3/5) SCHEMATIC DIAGRAM



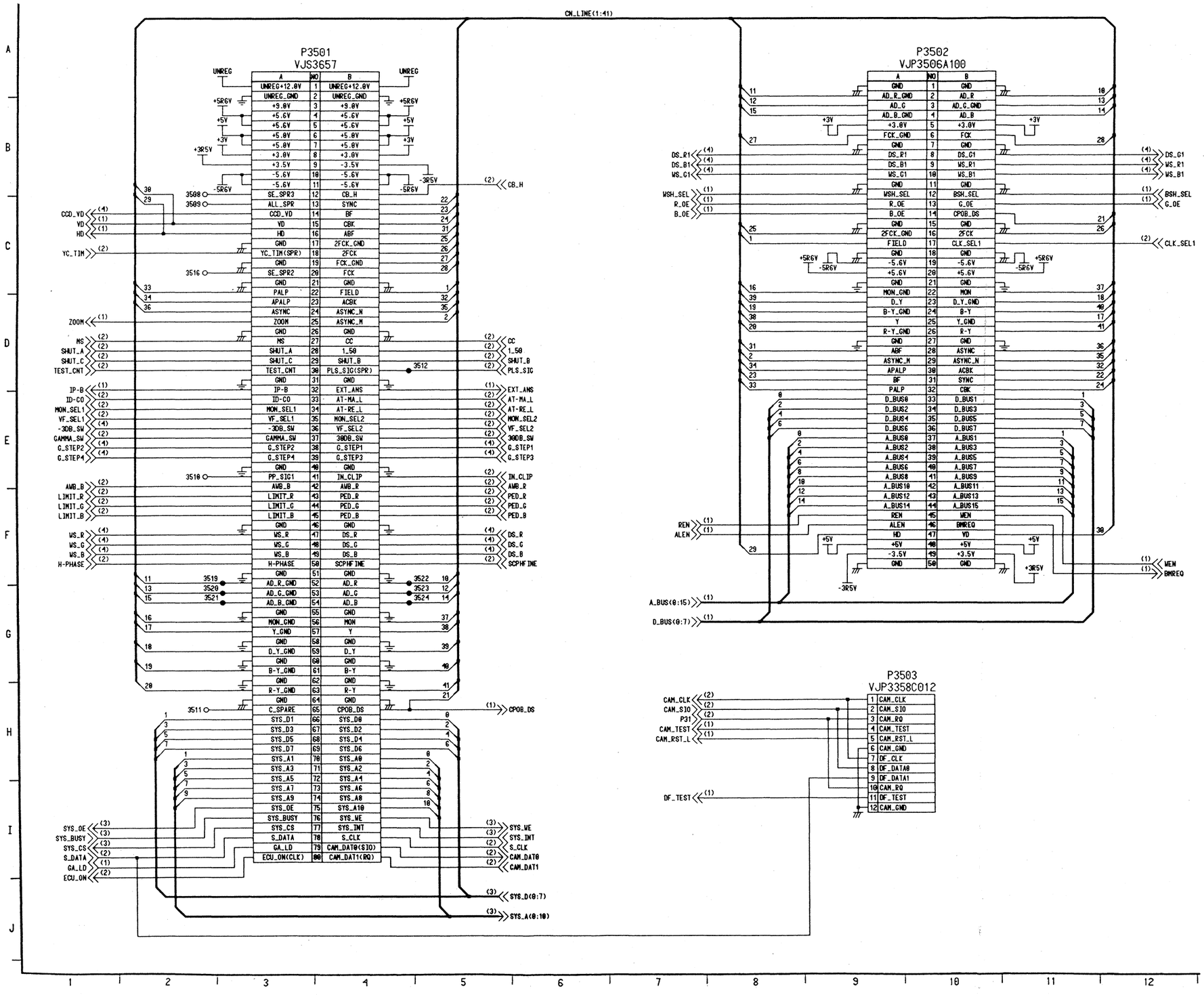
2—15

CAMERA SYSCON (4/5) SCHEMATIC DIAGRAM



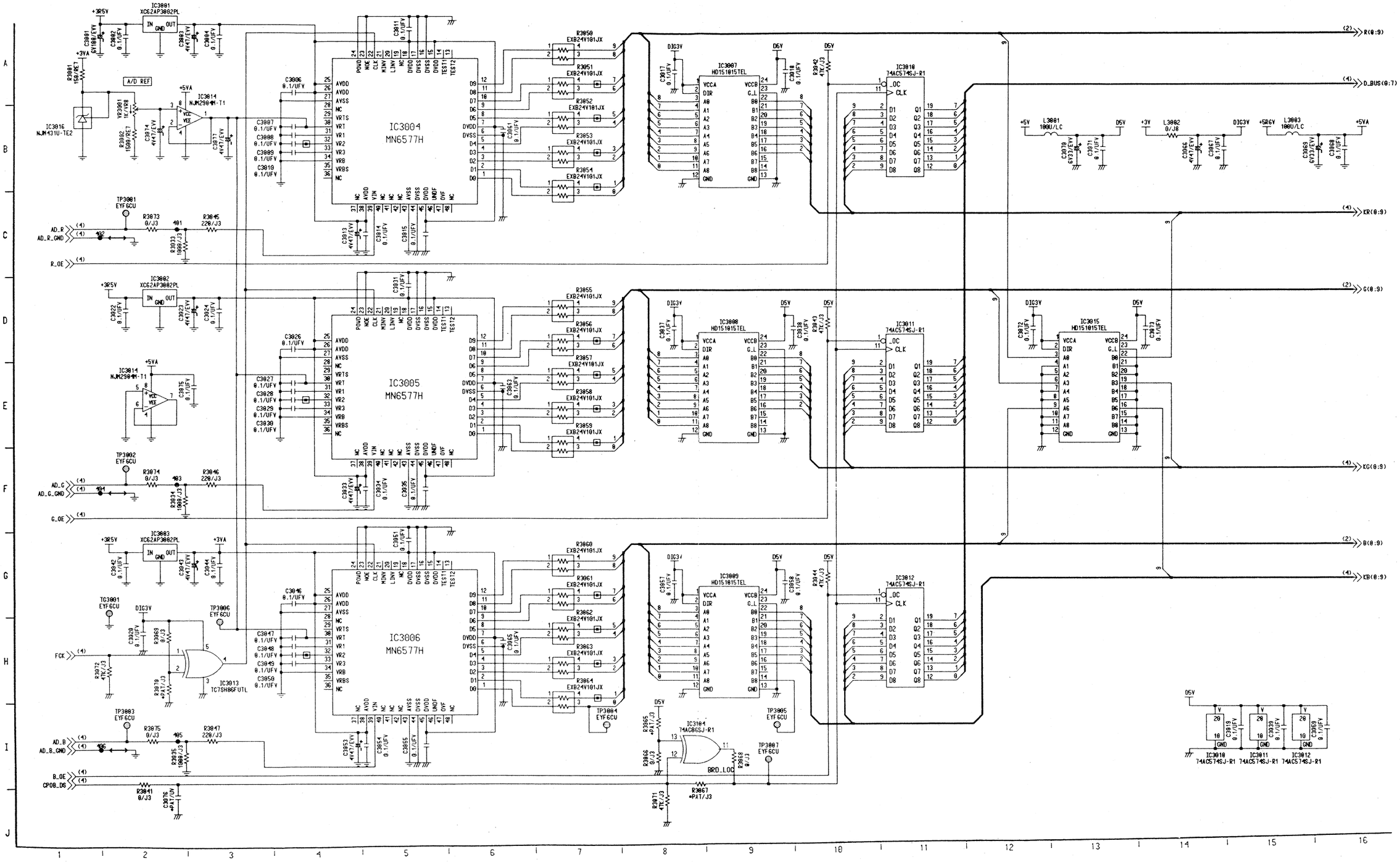
2—16

CAMERA SYSCON (5/5) SCHEMATIC DIAGRAM

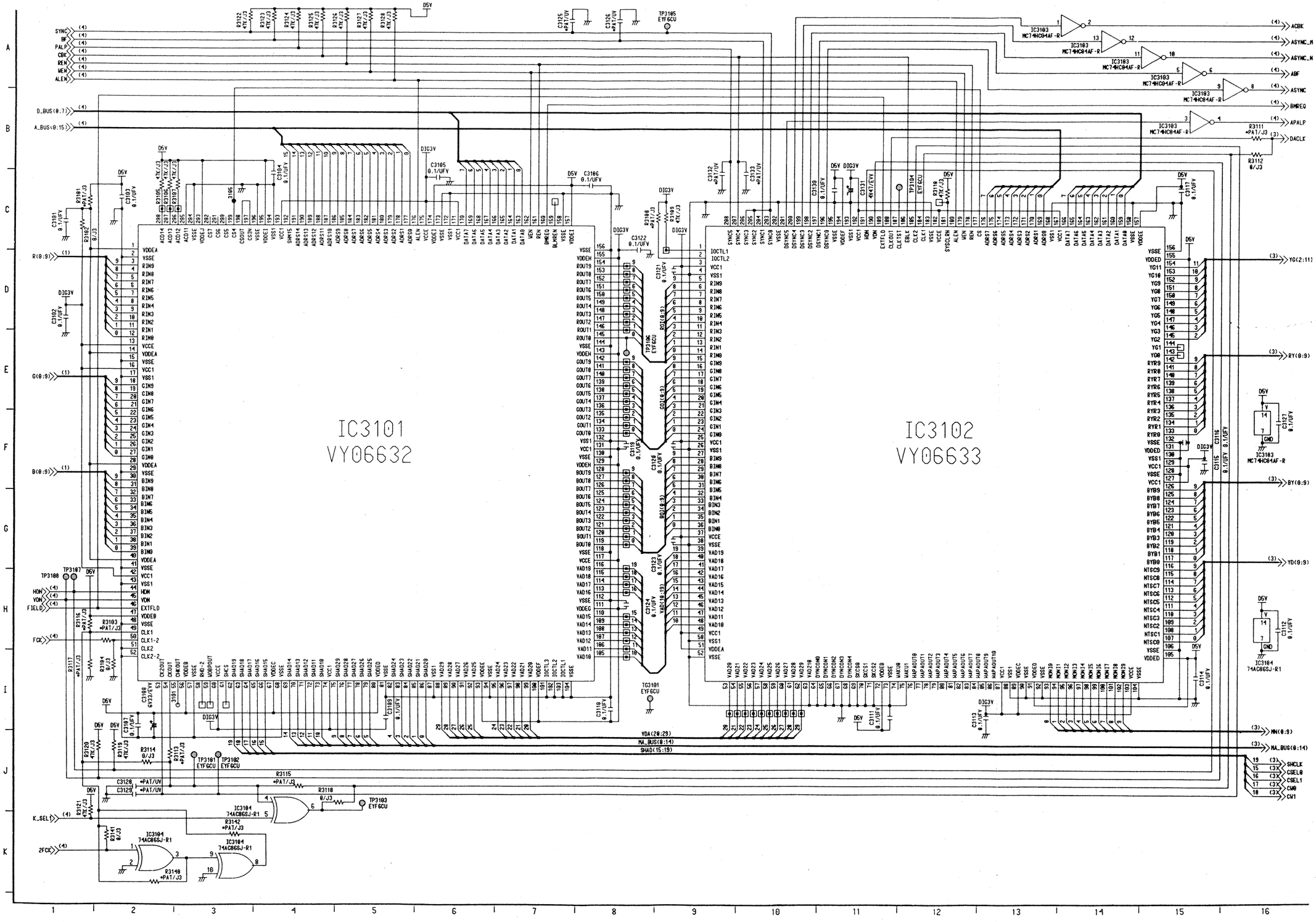


2—17

CAMERA DSP (1/4) SCHEMATIC DIAGRAM

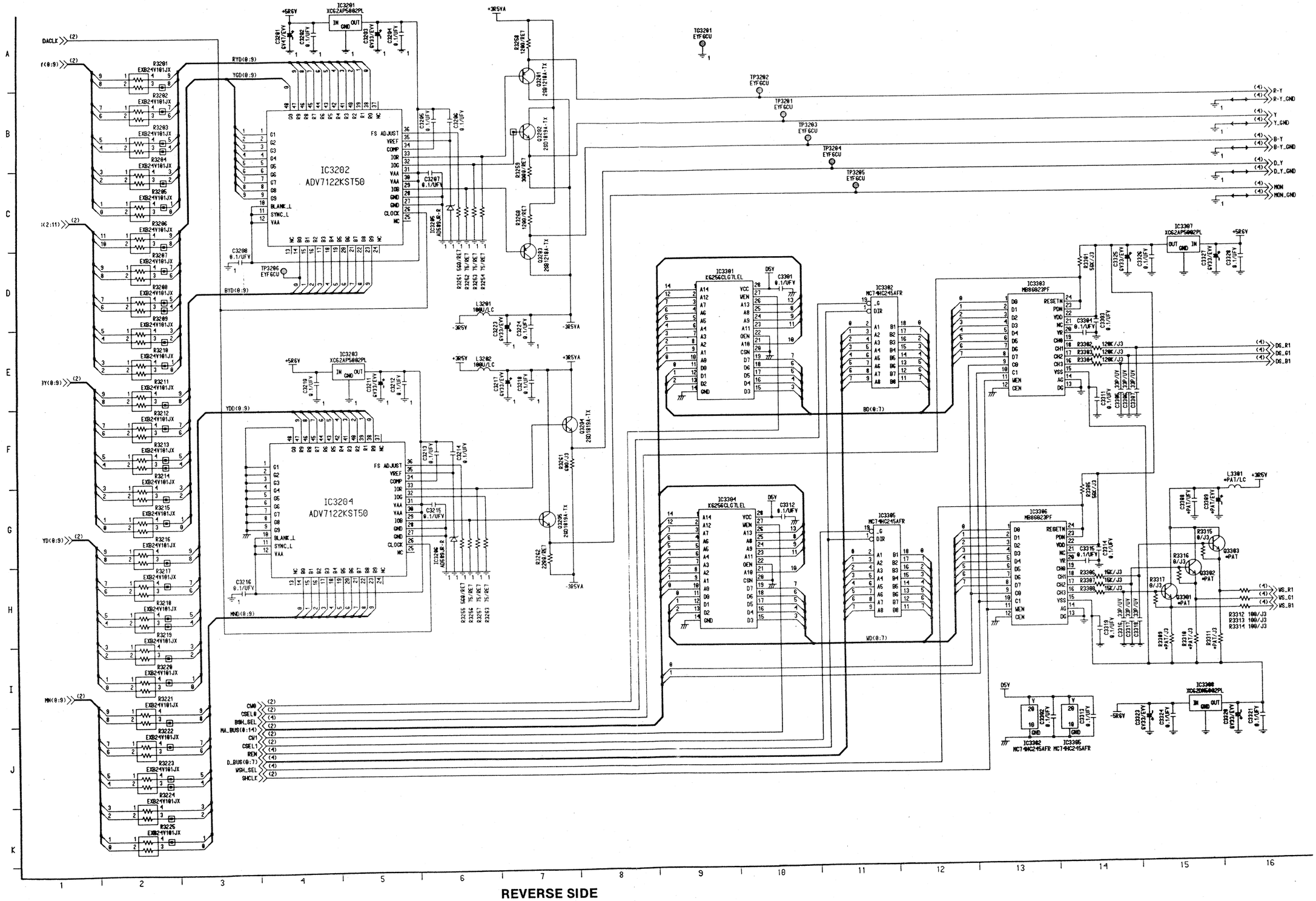


CAMERA DSP (2/4) SCHEMATIC DIAGRAM



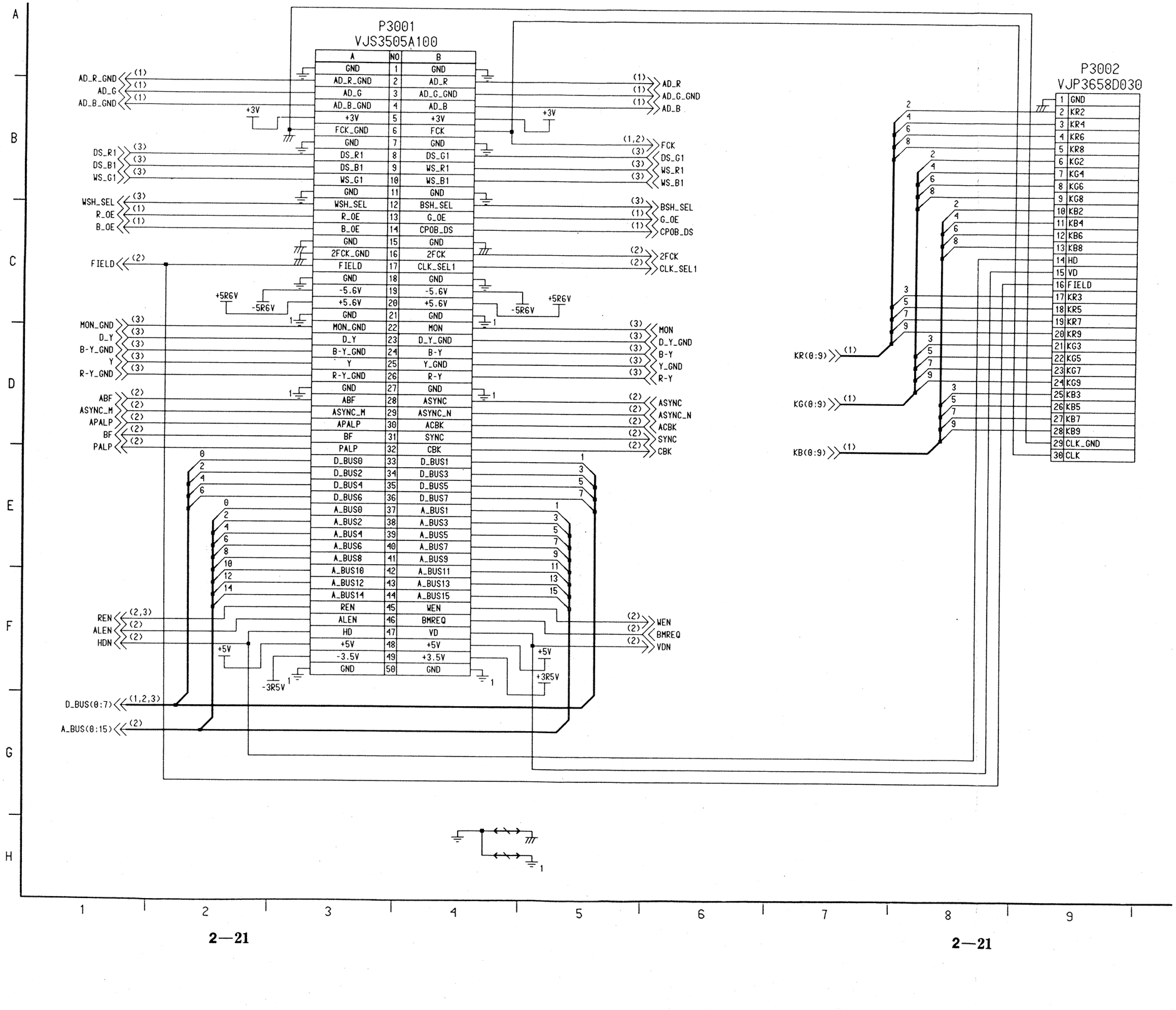
2—19

CAMERA DSP (3/4) SCHEMATIC DIAGRAM



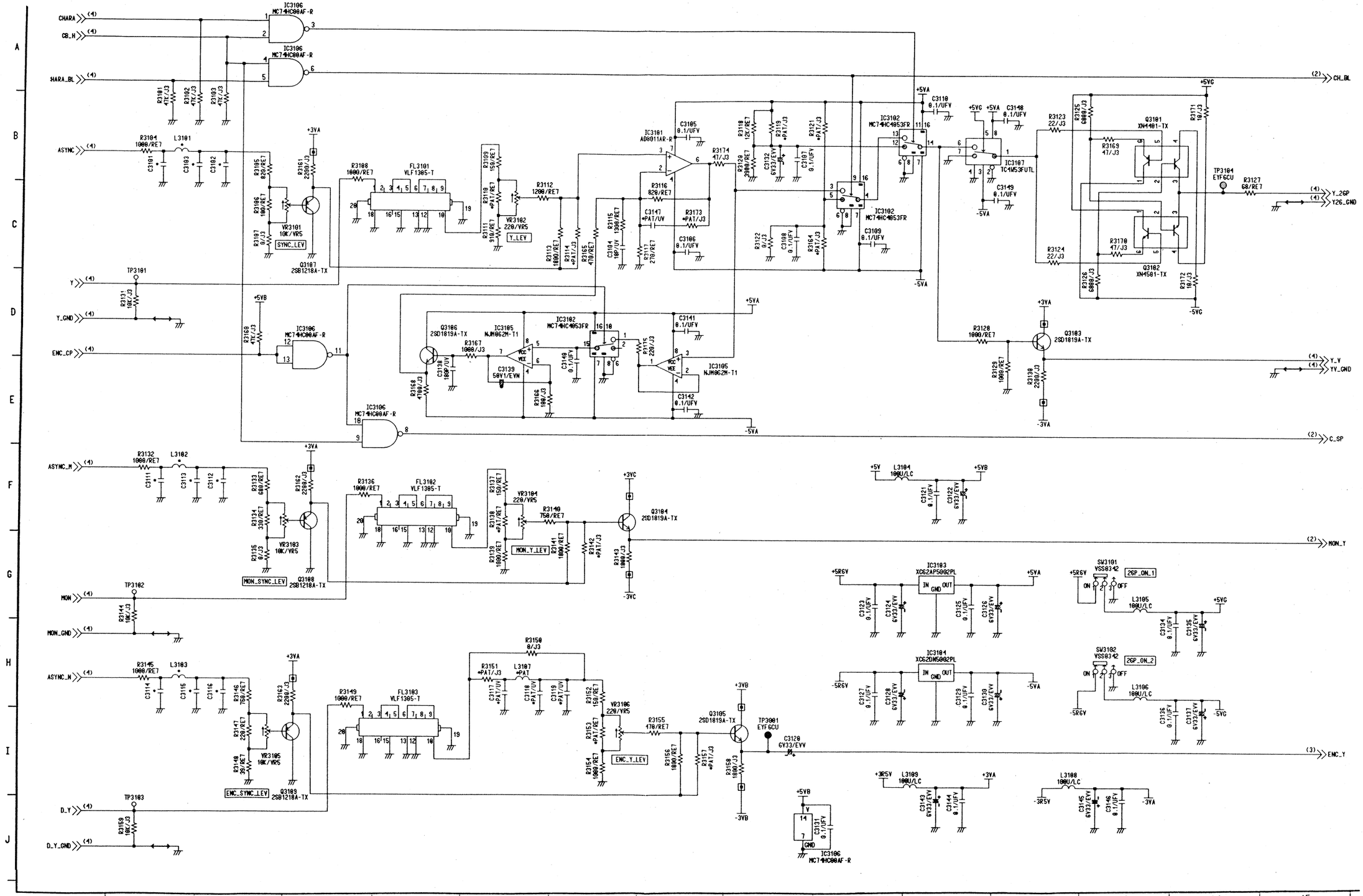
REVERSE SIDE

CAMERA DSP (4/4) CONNECTOR SCHEMATIC DIAGRAM



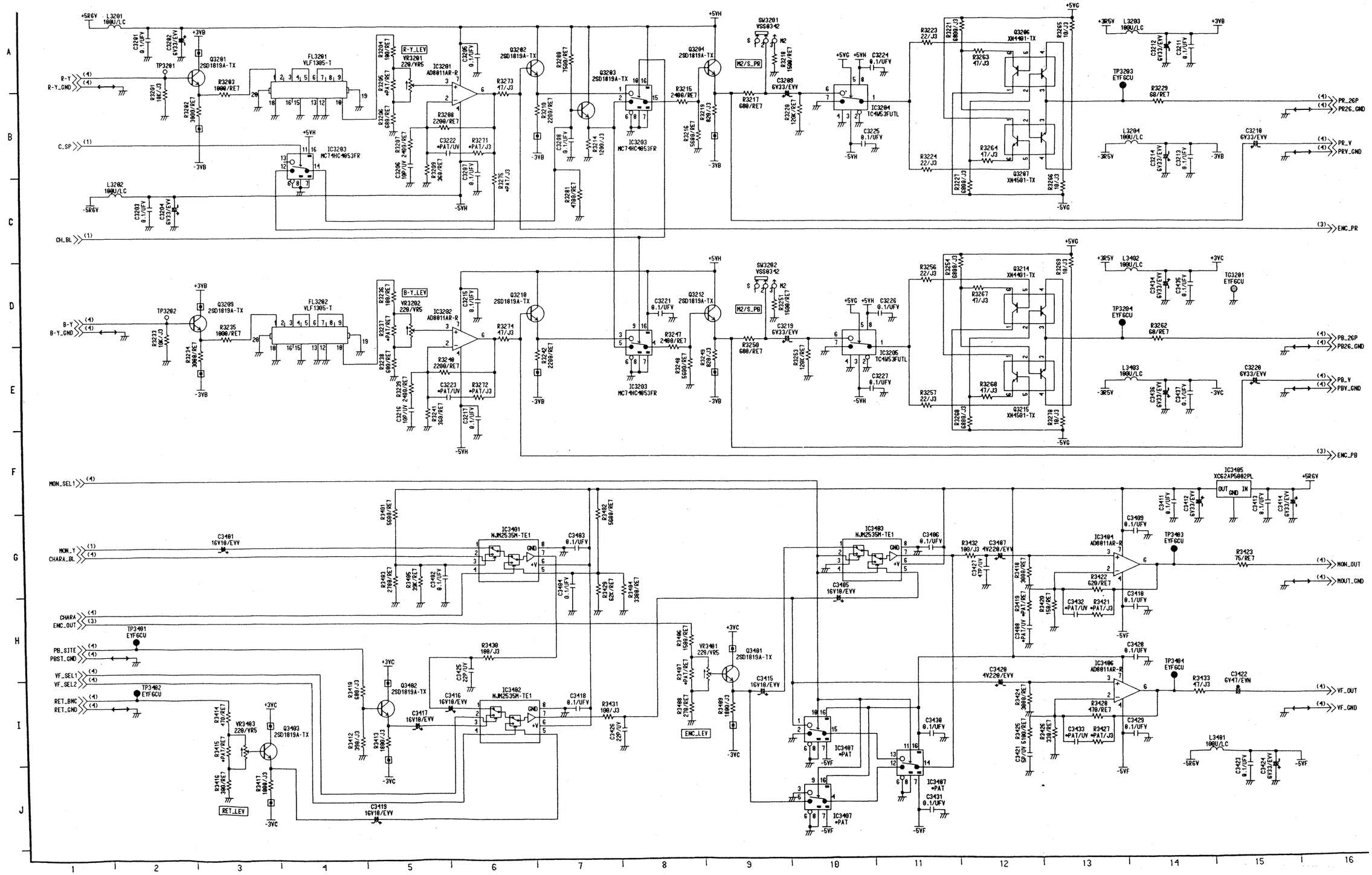
2—21

CAMERA ENCODER (1/7) SCHEMATIC DIAGRAM



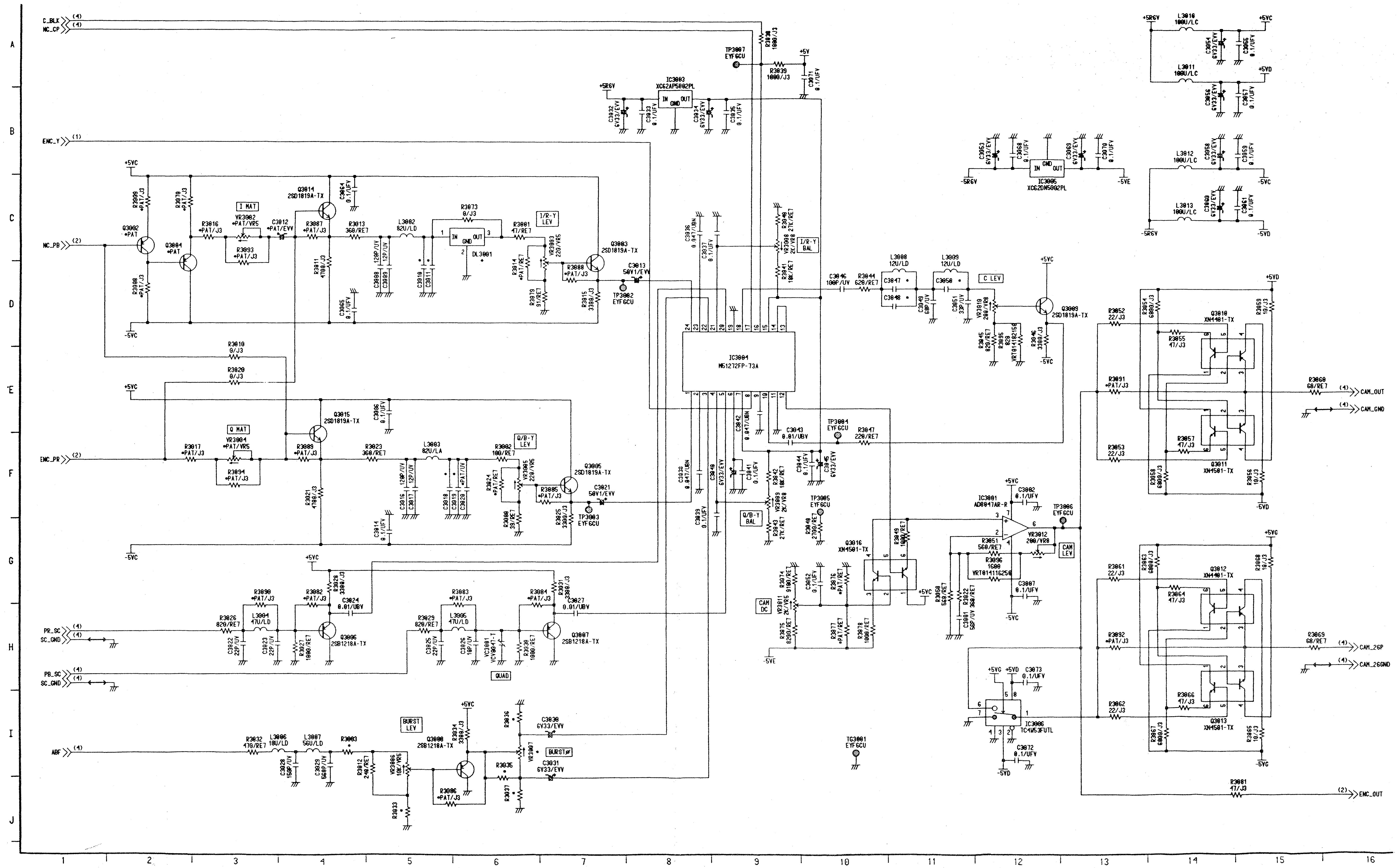
REVERSE SIDE

CAMERA ENCODER (2/7) SCHEMATIC DIAGRAM



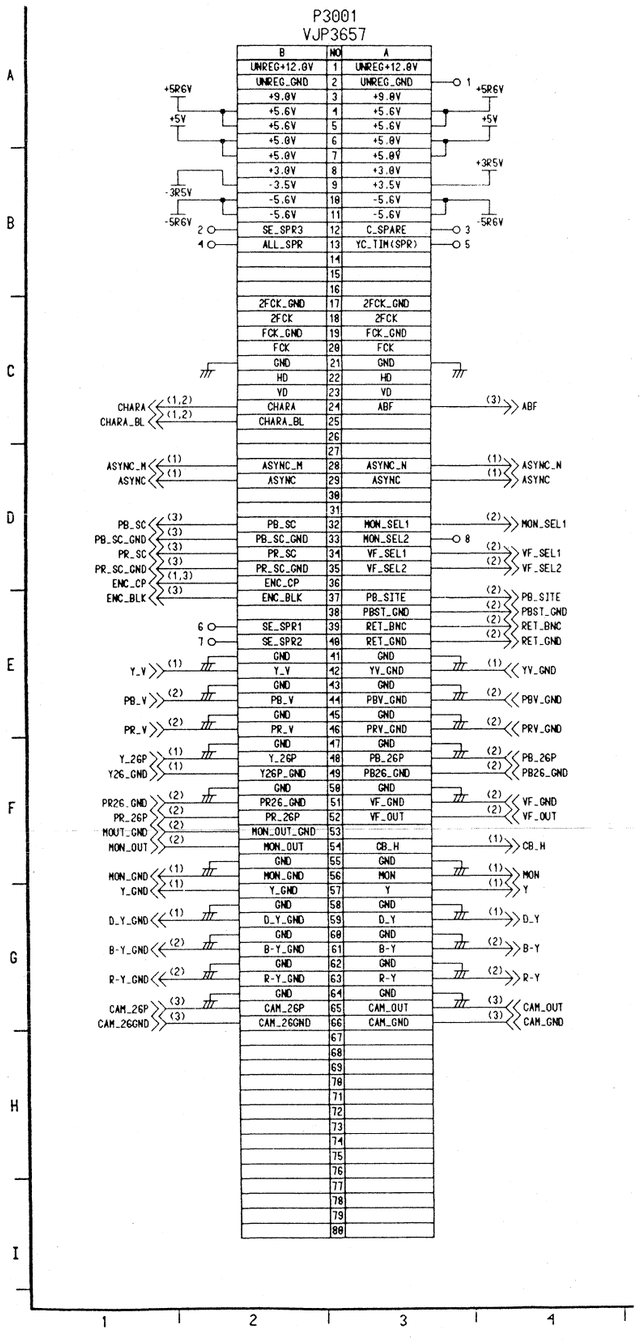
2—23

CAMERA ENCODER (3/7) SCHEMATIC DIAGRAM



REVERSE SIDE
CAMERA ENCODER 2/7

CAMERA ENCODER (4/7)
CONNECTOR SCHEMATIC DIAGRAM



CAMERA ENCODER (5/7)
COMPARISON CHART 1 BETWEEN MODELS

REF	NTSC	PAL	ON
C3010	56P/UV	100P/UV	56P/UV
C3011	33P/UV	15P/UV	33P/UV
C3012	*PAT/EVV	*PAT/EVV	6V33/EVV
C3018	56P/UV	100P/UV	680P/USV
C3019	33P/UV	15P/UV	330P/UV
C3020	*PAT/UV	*PAT/UV	9P/UV
C3047	3P/UV	2P/UV	3P/UV
C3048	33P/UV	18P/UV	33P/UV
C3050	18P/UV	9P/UV	18P/UV
C3101	8P/UV	22P/UV	18P/UV
C3102	100P/UV	180P/UV	120P/UV
C3103	*PAT/UV	33P/UV	12P/UV
C3111	8P/UV	22P/UV	18P/UV
C3112	100P/UV	180P/UV	120P/UV
C3113	*PAT/UV	33P/UV	12P/UV
C3114	8P/UV	22P/UV	18P/UV
C3115	100P/UV	180P/UV	120P/UV
C3116	*PAT/UV	33P/UV	12P/UV
C3117	*PAT/UV	*PAT/UV	18P/UV
C3118	*PAT/UV	*PAT/UV	18P/UV
C3119	*PAT/UV	*PAT/UV	1P/UV
C3147	*PAT/UV	*PAT/UV	27P/UV
C3222	*PAT/UV	*PAT/UV	27P/UV
C3223	*PAT/UV	*PAT/UV	27P/UV
C3408	*PAT/UV	*PAT/UV	12P/UV
C3432	*PAT/UV	*PAT/UV	27P/UV
C3433	*PAT/UV	*PAT/UV	27P/UV
DL3001	*PAT	*PAT	ELB4M087
IC3407	*PAT	*PAT	MC74HC4053FR
L3101	47U/LD	100U/LD	47U/LD
L3102	47U/LD	100U/LD	47U/LD
L3103	47U/LD	100U/LD	47U/LD
L3107	*PAT	*PAT	39U/LD
Q3002	*PAT	*PAT	2SB1218A-TX
Q3004	*PAT	*PAT	2SB1218A-TX
R3003	110/RE7	0/J3	110/RE7
R3008	*PAT/J3	*PAT/J3	560/J3
R3009	*PAT/J3	*PAT/J3	560/J3

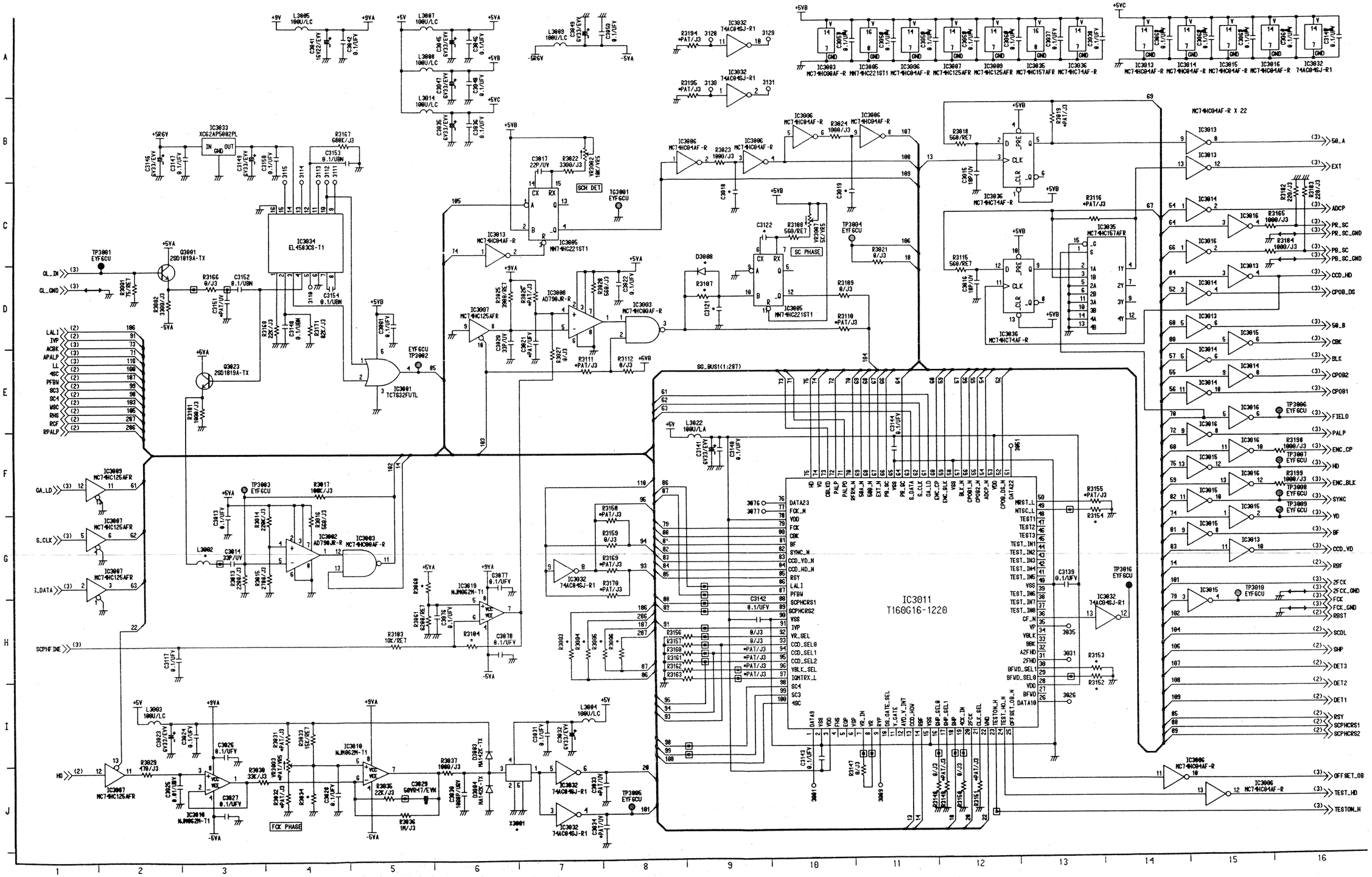
CAMERA ENCODER (6/7)
COMPARISON CHART 2 BETWEEN MODELS

REF	NTSC	PAL	ON
R3014	*PAT/RE7	*PAT/RE7	180/RE7
R3016	*PAT/J3	*PAT/J3	820/J3
R3017	*PAT/J3	*PAT/J3	820/J3
R3024	*PAT/RE7	*PAT/RE7	180/RE7
R3033	120/RE7	240/RE7	120/RE7
R3035	0/J3	*PAT/J3	0/J3
R3036	0/J3	*PAT/J3	0/J3
R3037	*PAT/J3	*PAT/J3	2200/J3
R3070	*PAT/J3	*PAT/J3	1000/J3
R3076	*PAT/RE7	*PAT/RE7	12K/RE7
R3077	*PAT/RE7	*PAT/RE7	8200/RE7
R3082	*PAT/J3	*PAT/J3	0/J3
R3083	*PAT/J3	*PAT/J3	0/J3
R3084	*PAT/J3	*PAT/J3	0/J3
R3085	*PAT/J3	*PAT/J3	0/J3
R3086	*PAT/J3	*PAT/J3	0/J3
R3087	*PAT/J3	*PAT/J3	0/J3
R3088	*PAT/J3	*PAT/J3	0/J3
R3089	*PAT/J3	*PAT/J3	0/J3
R3090	*PAT/J3	*PAT/J3	0/J3
R3091	*PAT/J3	*PAT/J3	0/J3
R3092	*PAT/J3	*PAT/J3	0/J3
R3093	*PAT/J3	*PAT/J3	0/J3
R3094	*PAT/J3	*PAT/J3	0/J3
R3110	*PAT/RE7	*PAT/RE7	220/RE7
R3114	*PAT/RE7	*PAT/RE7	220/RE7
R3119	*PAT/J3	*PAT/J3	1000/J3
R3121	*PAT/J3	*PAT/J3	1000/J3
R3138	*PAT/RE7	*PAT/RE7	240/RE7
R3142	*PAT/J3	*PAT/J3	1000/J3
R3151	*PAT/J3	*PAT/J3	0/J3
R3153	*PAT/RE7	*PAT/RE7	270/RE7
R3157	*PAT/J3	*PAT/J3	1000/J3
R3164	*PAT/J3	*PAT/J3	1000/J3
R3173	*PAT/J3	*PAT/J3	0/J3
R3205	*PAT/RE7	*PAT/RE7	220/RE7
R3237	*PAT/RE7	*PAT/RE7	220/RE7
R3271	*PAT/J3	*PAT/J3	0/J3

CAMERA ENCODER (7/7)
COMPARISON CHART 3 BETWEEN MODELS

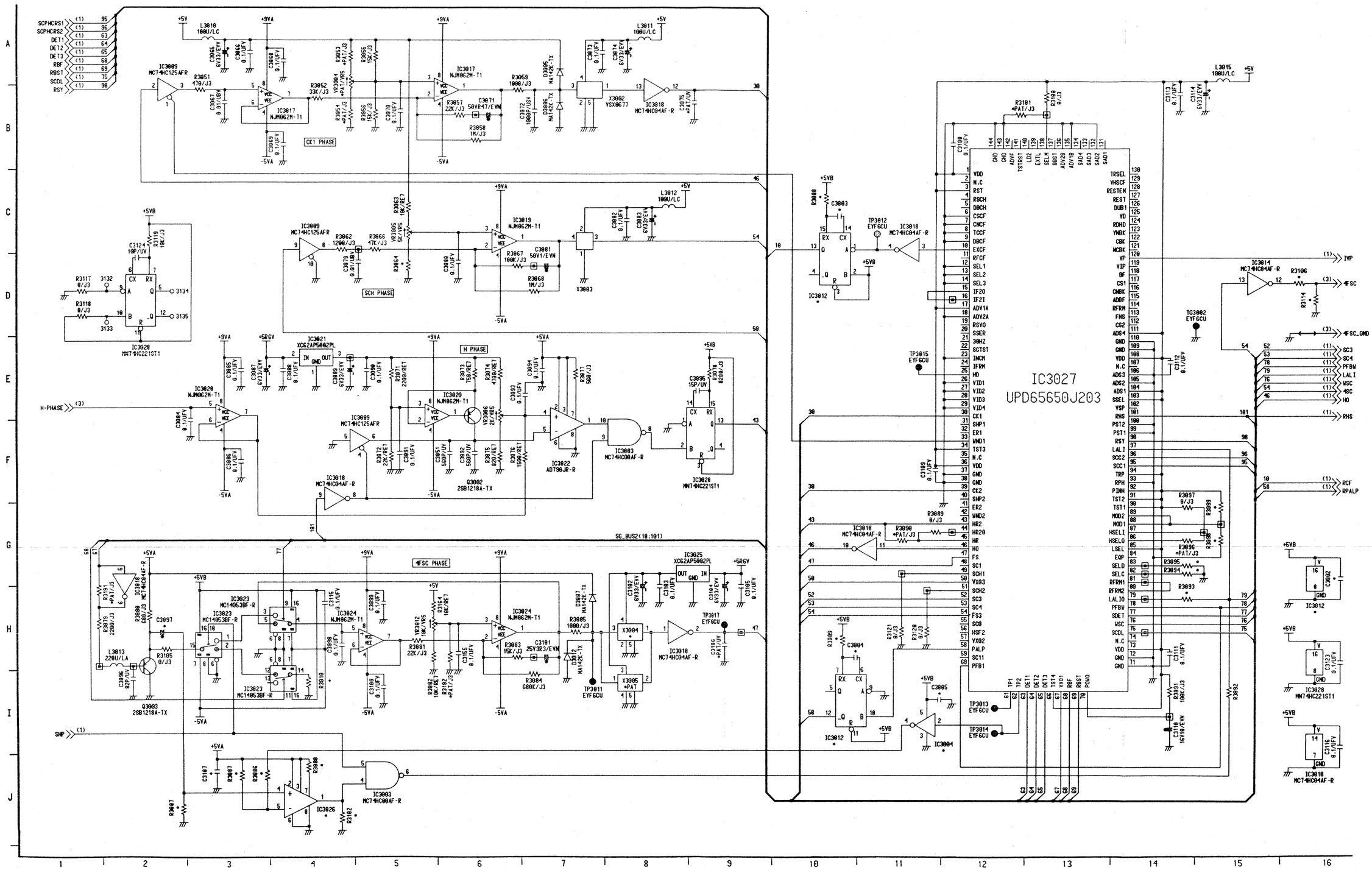
REF	NTSC	PAL	ON
R3272	*PAT/J3	*PAT/J3	0/J3
R3275	*PAT/J3	*PAT/J3	47/J3
R3407	*PAT/RE7	*PAT/RE7	220/RE7
R3415	*PAT/RE7	*PAT/RE7	220/RE7
R3419	*PAT/RE7	*PAT/RE7	2200/RE7
R3421	*PAT/J3	*PAT/J3	0/J3
R3427	*PAT/J3	*PAT/J3	0/J3
VR3002	*PAT/VR5	*PAT/VR5	1K/VR5
VR3004	*PAT/VR5	*PAT/VR5	1K/VR5
VR3007	*PAT/VR5	5K/VR5	5K/VR5

CAMERA SYNC (1/5) SCHEMATIC DIAGRAM



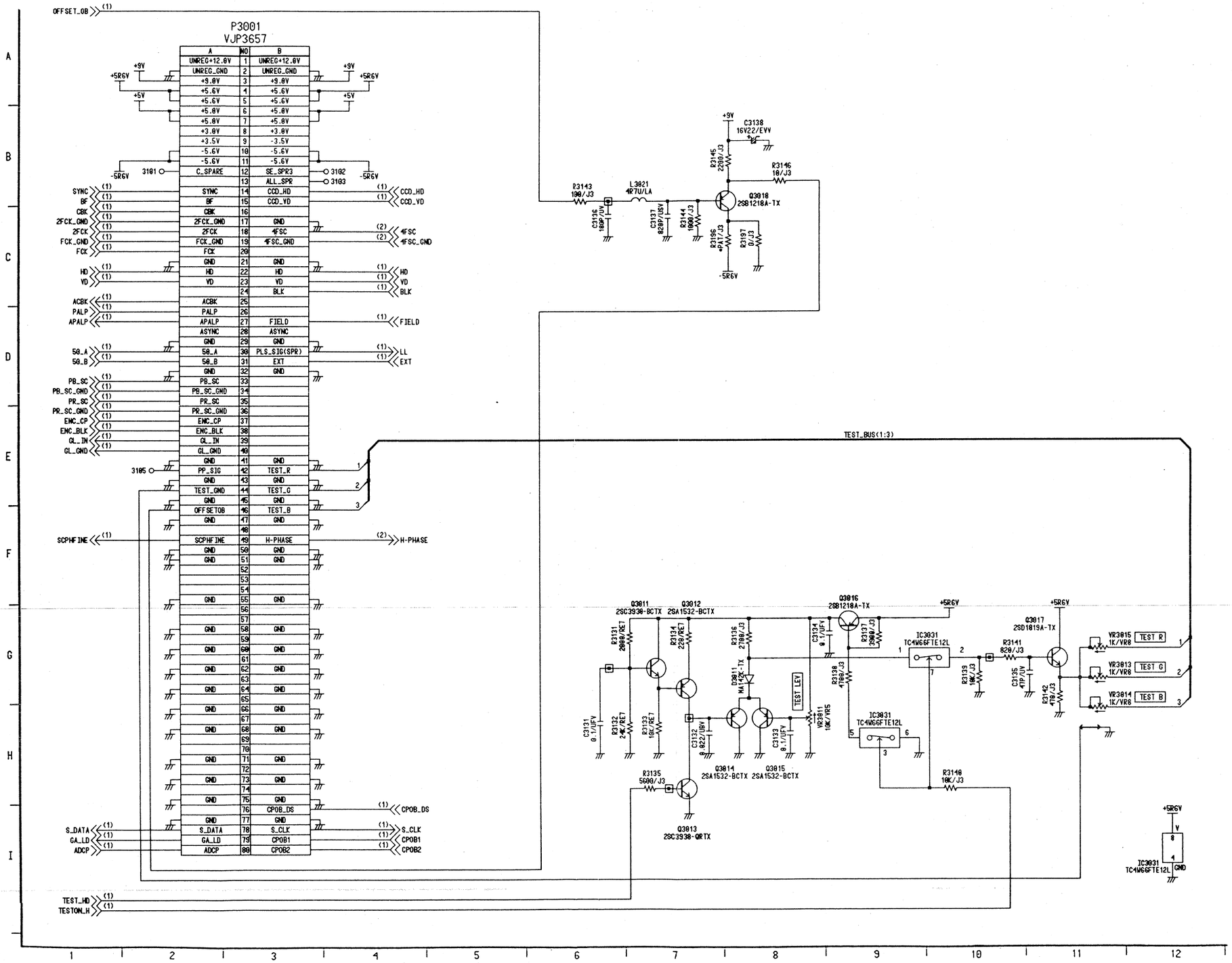
REVERSE SIDE

CAMERA SYNC (2/5) SCHEMATIC DIAGRAM



2—27

CAMERA SYNC (3/5) SCHEMATIC DIAGRAM



REVERSE SIDE

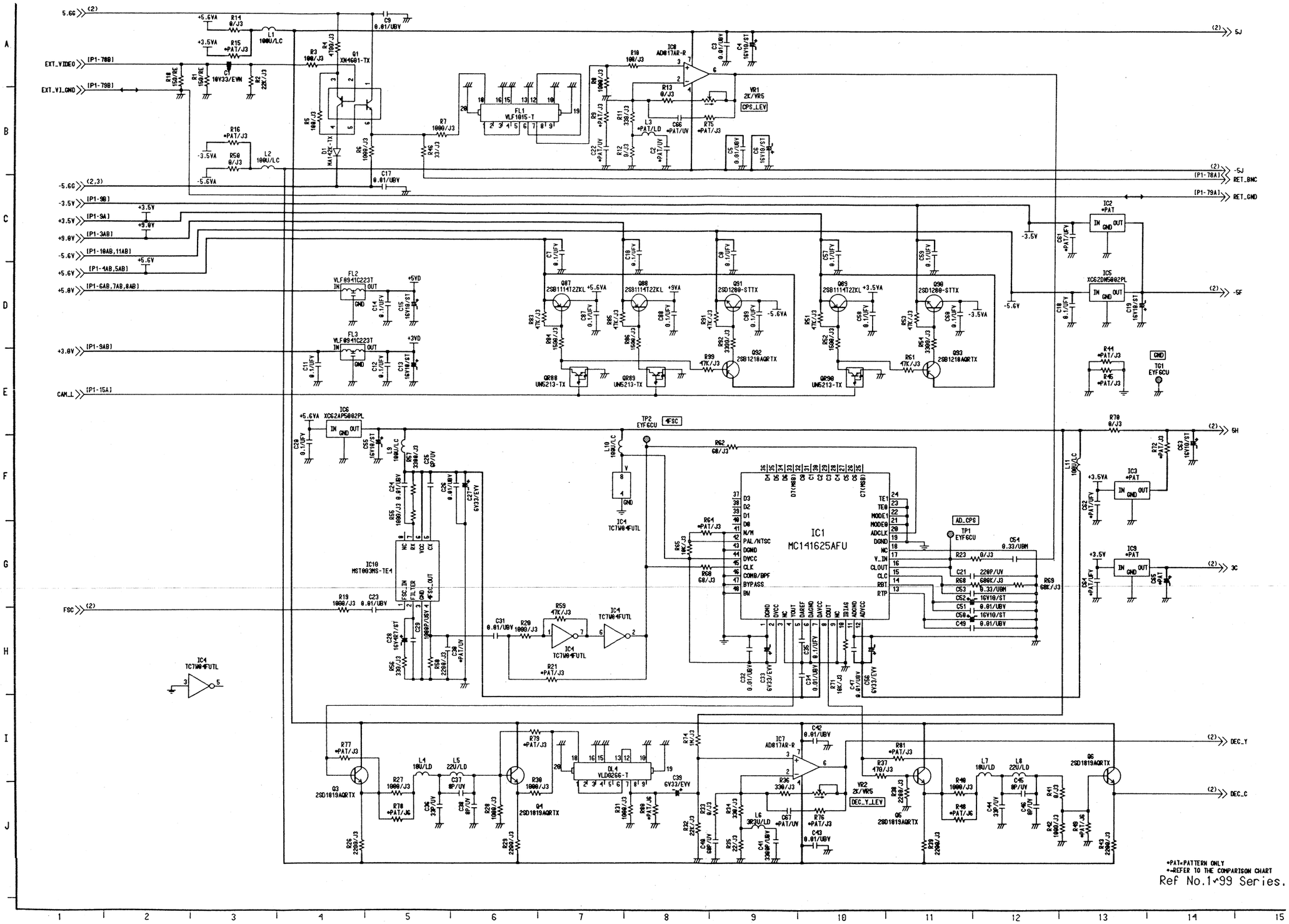
CAMERA SYNC (4/5)
COMPARISON CHART 1 BETWEEN MODELS

REF	NTSC	PAL	ON
C3002	*PAT/UFV	0. 1/UFV	0. 1/UFV
C3003	*PAT/UV	10P/UV	10P/UV
C3004	*PAT/UV	150P/UV	150P/UV
C3005	*PAT/UFV	0. 1/UFV	0. 1/UFV
C3018	15P/UV	*PAT/UV	15P/UV
C3019	15P/UV	*PAT/UV	15P/UV
C3021	*PAT/UFV	*PAT/UFV	0. 1/UFV
C3033	*PAT/UV	*PAT/UV	10P/UV
C3034	*PAT/UV	*PAT/UV	10P/UV
C3075	*PAT/UV	*PAT/UV	10P/UV
C3097	*PAT/EVN	16V10/EVN	16V10/EVN
C3106	*PAT/UV	*PAT/UV	10P/UV
C3107	*PAT/UFV	0. 1/UFV	0. 1/UFV
C3121	10P/UV	*PAT/UV	10P/UV
C3122	22P/UV	12P/UV	22P/UV
C3151	*PAT/UV	*PAT/UV	470P/UV
D3008	MA142K-TX	*PAT	MA142K-TX
IC3004	*PAT	TC7S04FUTL	TC7S04FUTL
IC3012	*PAT	MN74HC221ST1	MN74HC221ST1
IC3026	*PAT	AD790JR-R	AD790JR-R
L3002	68U/LA	39U/LA	68U/LA
R3003	0/J3	*PAT/J3	0/J3
R3004	*PAT/J3	0/J3	0/J3
R3005	0/J3	*PAT/J3	0/J3
R3006	*PAT/J3	0/J3	0/J3
R3007	*PAT/J3	10K/J3	10K/J3
R3008	*PAT/J3	15K/J3	15K/J3
R3009	*PAT/J3	270K/J3	270K/J3
R3010	0/J3	*PAT/J3	0/J3
R3019	*PAT/J3	*PAT/J3	6800/J3
R3026	*PAT/J3	*PAT/J3	12K/J3
R3031	*PAT/J3	*PAT/J3	10K/J3
R3032	*PAT/J3	*PAT/J3	10K/J3
R3034	16K/RE7	20K/RE7	16K/RE7
R3053	*PAT/J3	*PAT/J3	10K/J3
R3054	*PAT/J3	*PAT/J3	10K/J3
R3060	9100/RE7	10K/RE7	9100/RE7
R3064	13K/RE7	18K/RE7	13K/RE7
R3086	*PAT/J3	4700/J3	4700/J3
R3087	*PAT/J3	18K/J3	18K/J3
R3088	*PAT/J3	560/J3	560/J3
R3090	*PAT/J3	*PAT/J3	0/J3
R3092	*PAT/J3	0/J3	0/J3

CAMERA SYNC (5/5)
COMPARISON CHART 2 BETWEEN MODELS

REF	NTSC	PAL	ON
R3093	0/J3	*PAT/J3	0/J3
R3094	*PAT/J3	0/J3	0/J3
R3095	*PAT/J3	0/J3	0/J3
R3096	*PAT/J3	*PAT/J3	0/J3
R3098	0/J3	*PAT/J3	0/J3
R3099	*PAT/J3	0/J3	0/J3
R3101	*PAT/J3	*PAT/J3	0/J3
R3102	0/J3	*PAT/J3	0/J3
R3104	5600/RE7	4700/RE7	5600/RE7
R3106	*PAT/J3	1000/J3	1000/J3
R3107	820/RE7	0/J3	820/RE7
R3110	*PAT/J3	*PAT/J3	0/J3
R3111	*PAT/J3	*PAT/J3	0/J3
R3114	*PAT/J3	1000/J3	1000/J3
R3116	*PAT/J3	*PAT/J3	0/J3
R3149	*PAT/J3	*PAT/J3	0/J3
R3151	*PAT/J3	*PAT/J3	0/J3
R3152	0/J3	*PAT/J3	0/J3
R3153	*PAT/J3	0/J3	0/J3
R3154	0/J3	*PAT/J3	0/J3
R3155	*PAT/J3	*PAT/J3	0/J3
R3158	*PAT/J3	*PAT/J3	0/J3
R3160	*PAT/J3	*PAT/J3	0/J3
R3161	*PAT/J3	*PAT/J3	0/J3
R3162	*PAT/J3	*PAT/J3	0/J3
R3163	*PAT/J3	*PAT/J3	0/J3
R3169	*PAT/J3	*PAT/J3	0/J3
R3170	*PAT/J3	*PAT/J3	0/J3
R3191	*PAT/J3	*PAT/J3	0/J3
R3192	*PAT/J3	*PAT/J3	18K/J3
R3194	*PAT/J3	*PAT/J3	0/J3
R3195	*PAT/J3	*PAT/J3	0/J3
R3196	*PAT/J3	*PAT/J3	0/J3
VR3003	*PAT/VR5	*PAT/VR5	5K/VR5
VR3004	*PAT/VR5	*PAT/VR5	5K/VR5
X3001	VSX0686	VSX0687	VSX0686
X3003	VSX0338	VSX0270	VSX0338
X3004	VSX0688	VSX0689	VSX0688
X3005	*PAT	*PAT	VSX0332

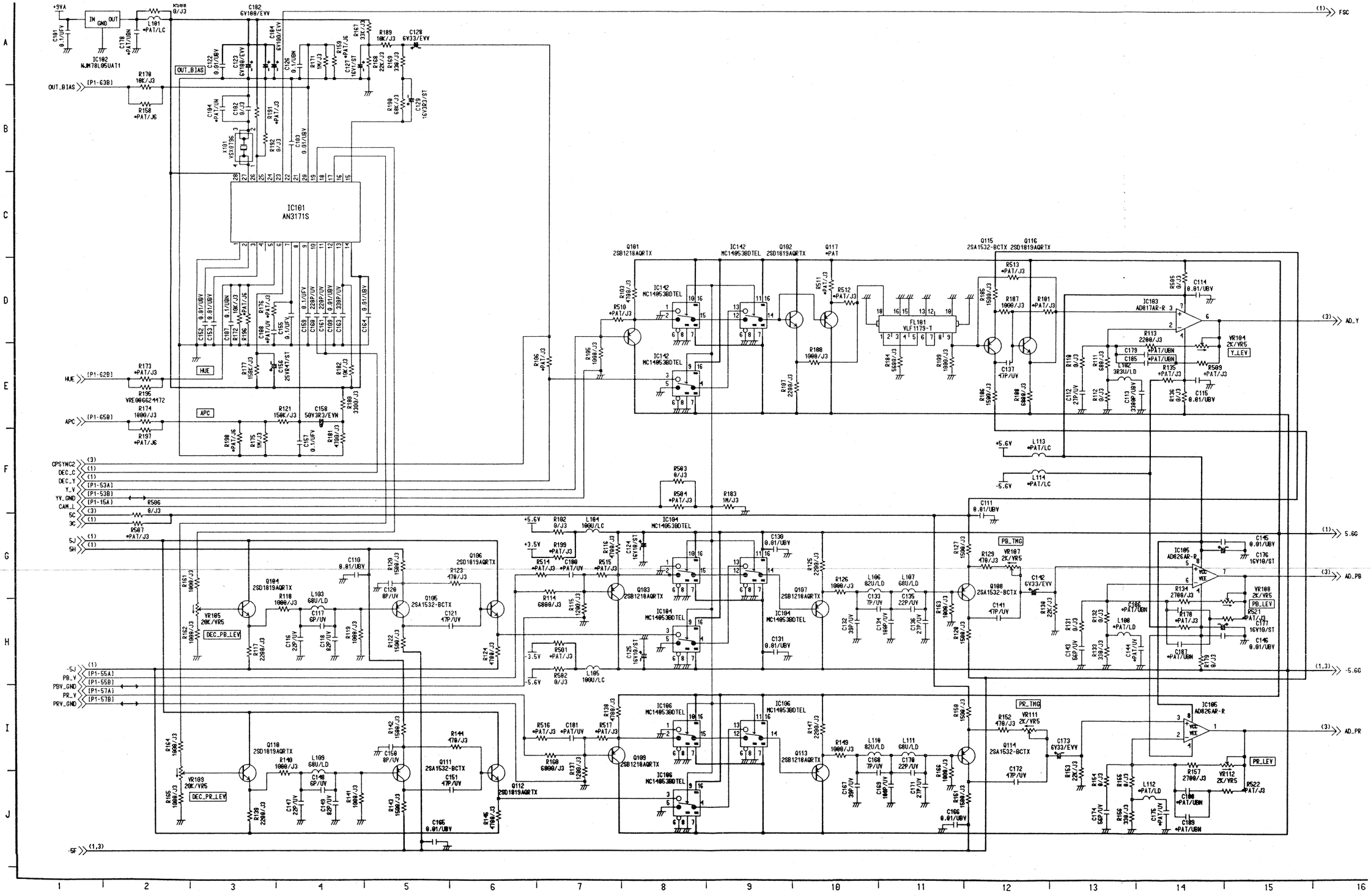
VIDEO IF (1/5) SCHEMATIC DIAGRAM



REVERSE SIDE

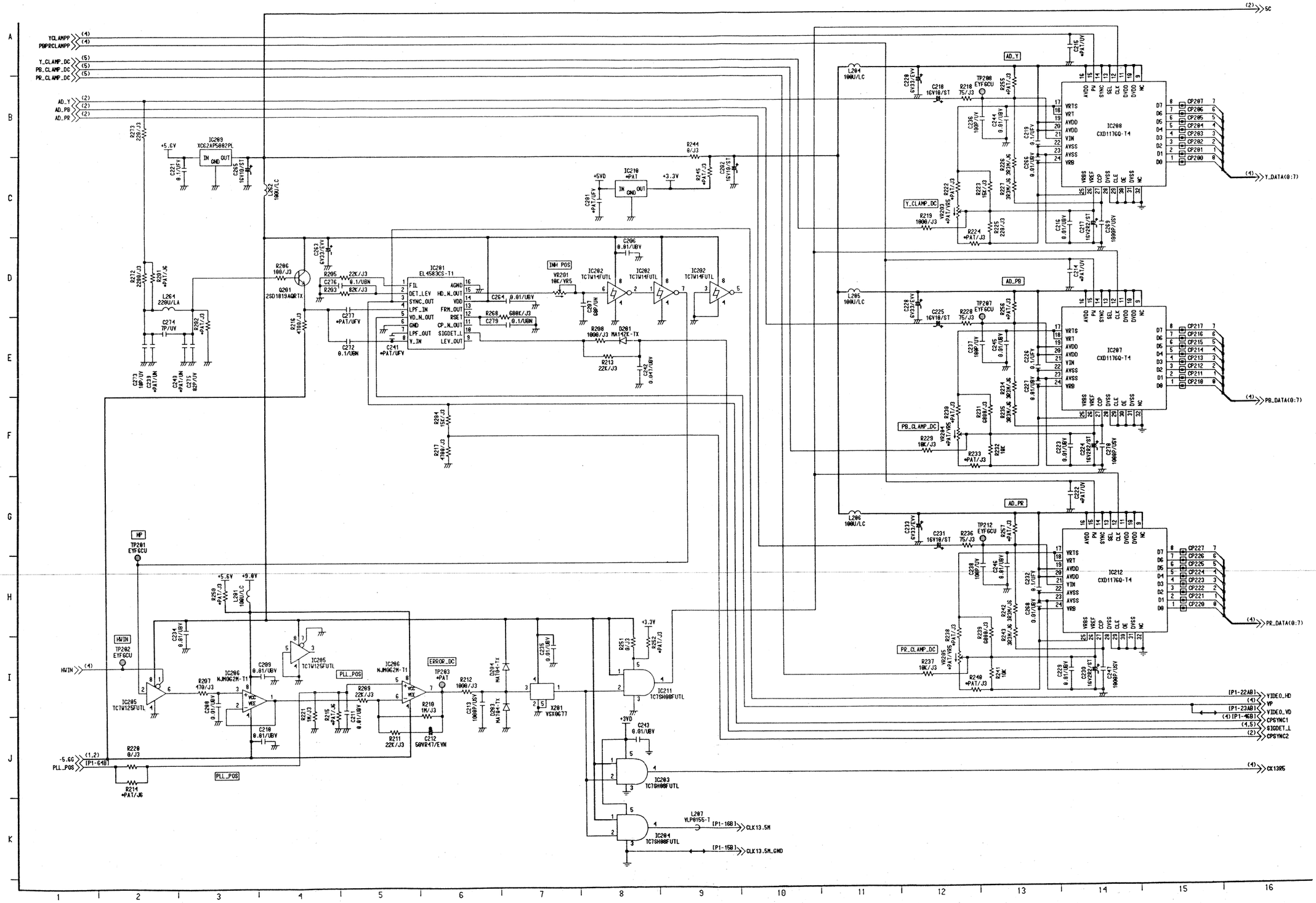
CAMERA SYNC 4/5, 5/5

VIDEO IF (2/5) SCHEMATIC DIAGRAM



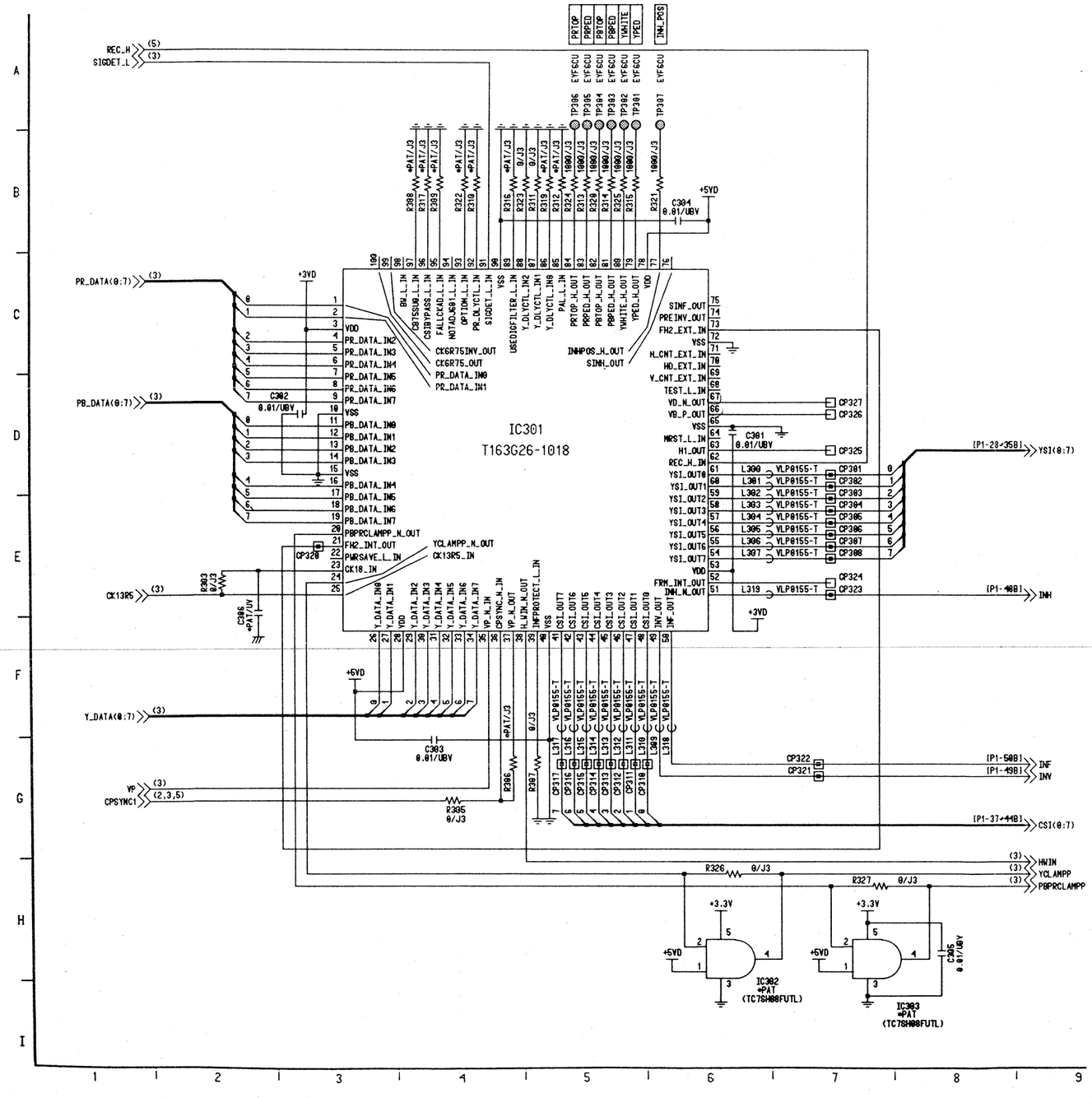
2—31

VIDEO IF (3/5) SCHEMATIC DIAGRAM

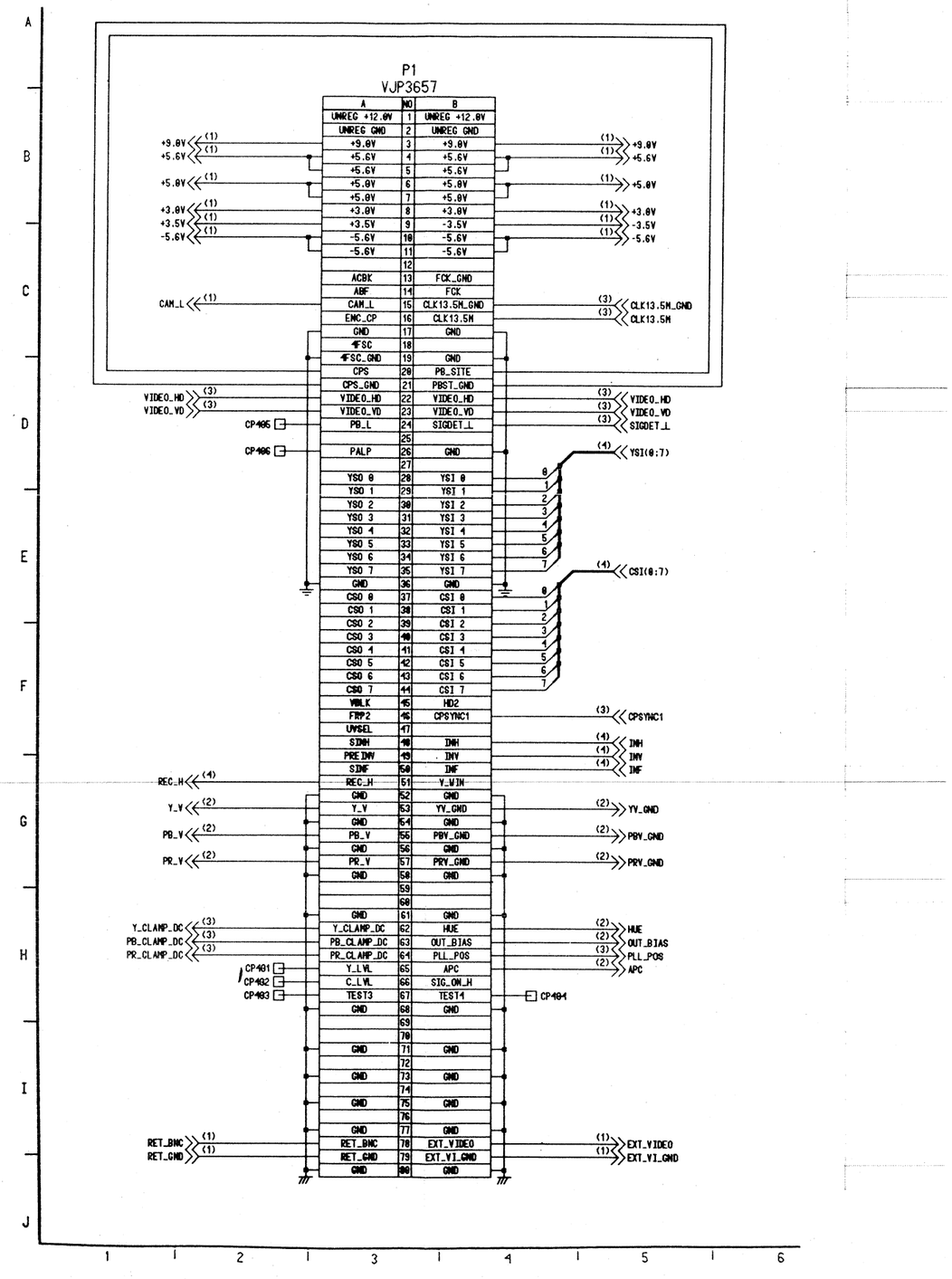


2—32

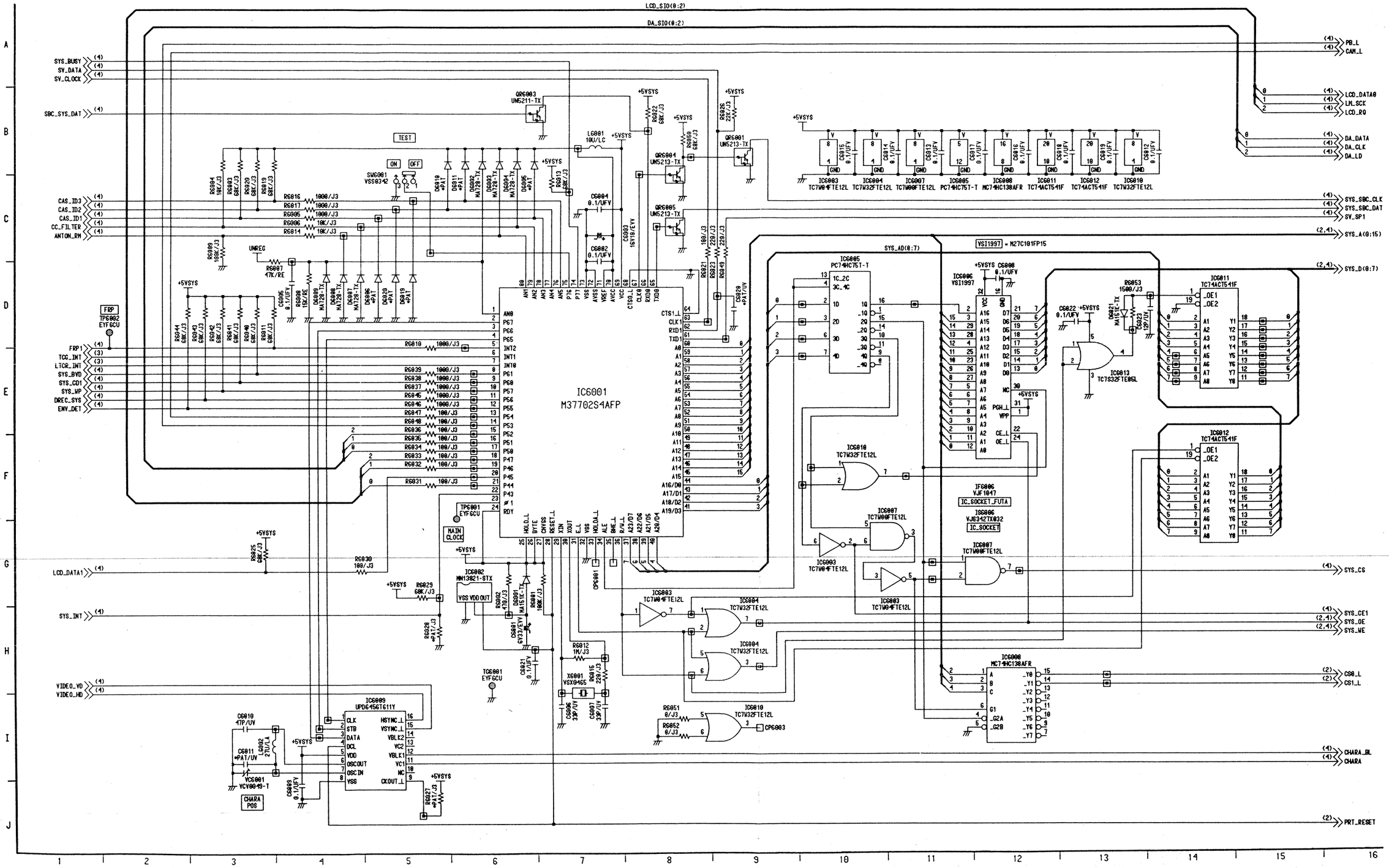
VIDEO IF (4/5) SCHEMATIC DIAGRAM



VIDEO IF (5/5) CONNECTOR SCHEMATIC DIAGRAM



VTR SYSCON (1/5) SCHEMATIC DIAGRAM

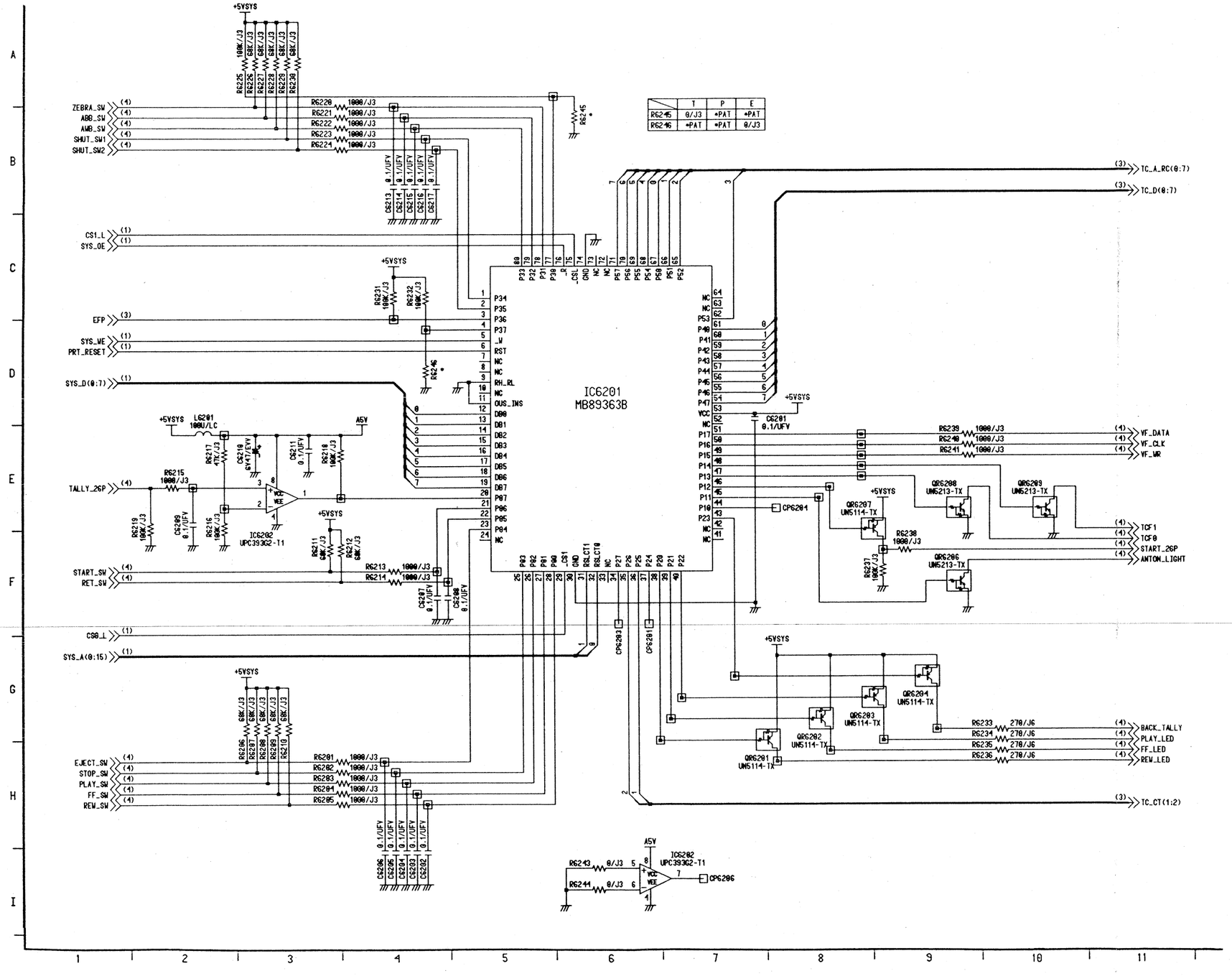


REVERSE SIDE

VIDEO IF 4/5, 5/5

2—34

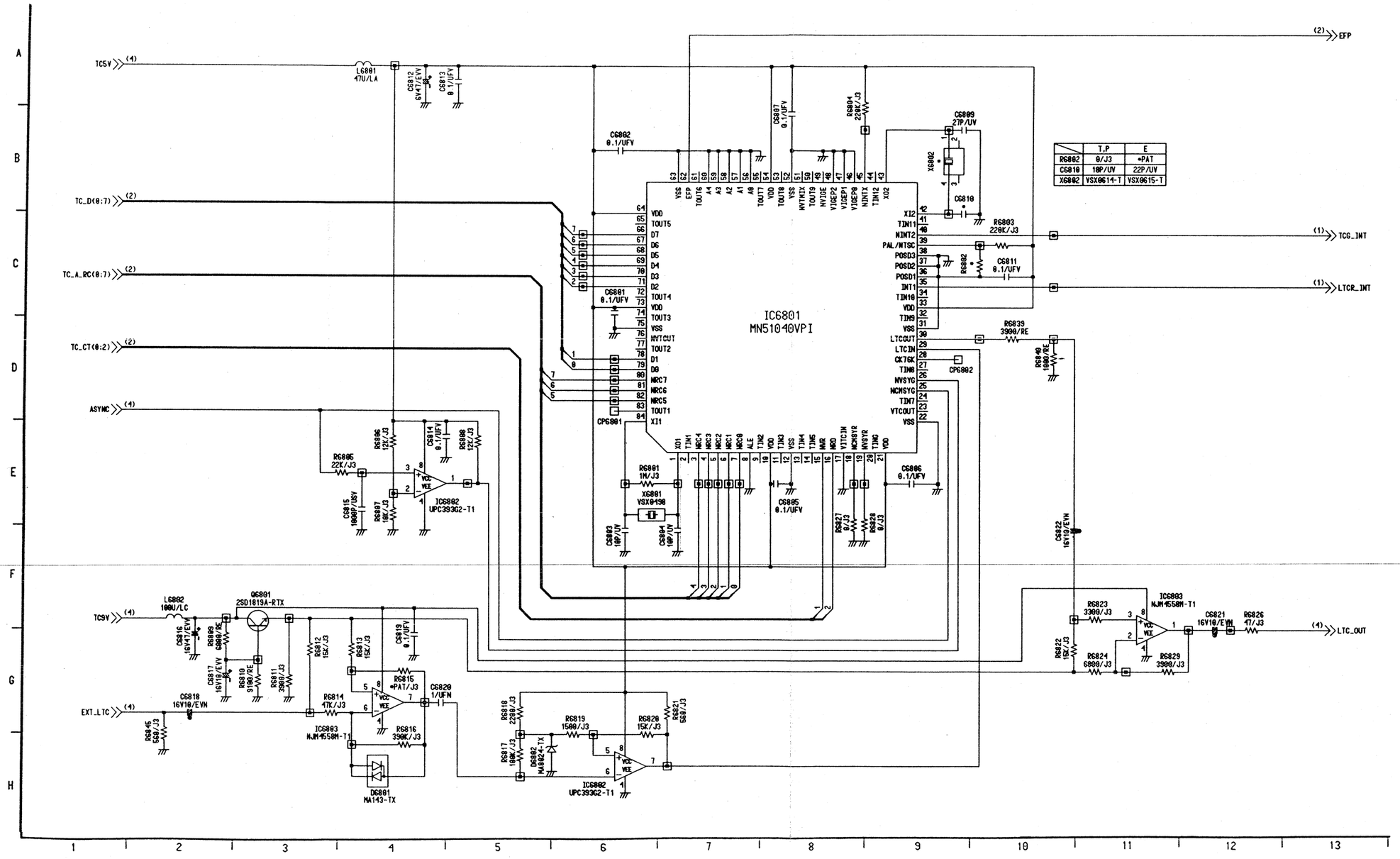
VTR SYSCON (2/5) SCHEMATIC DIAGRAM



	T	P	E
RG245	0/J3	*PAT	*PAT
RG246	*PAT	*PAT	0/J3

2—35

VTR SYSCON (3/5) SCHEMATIC DIAGRAM

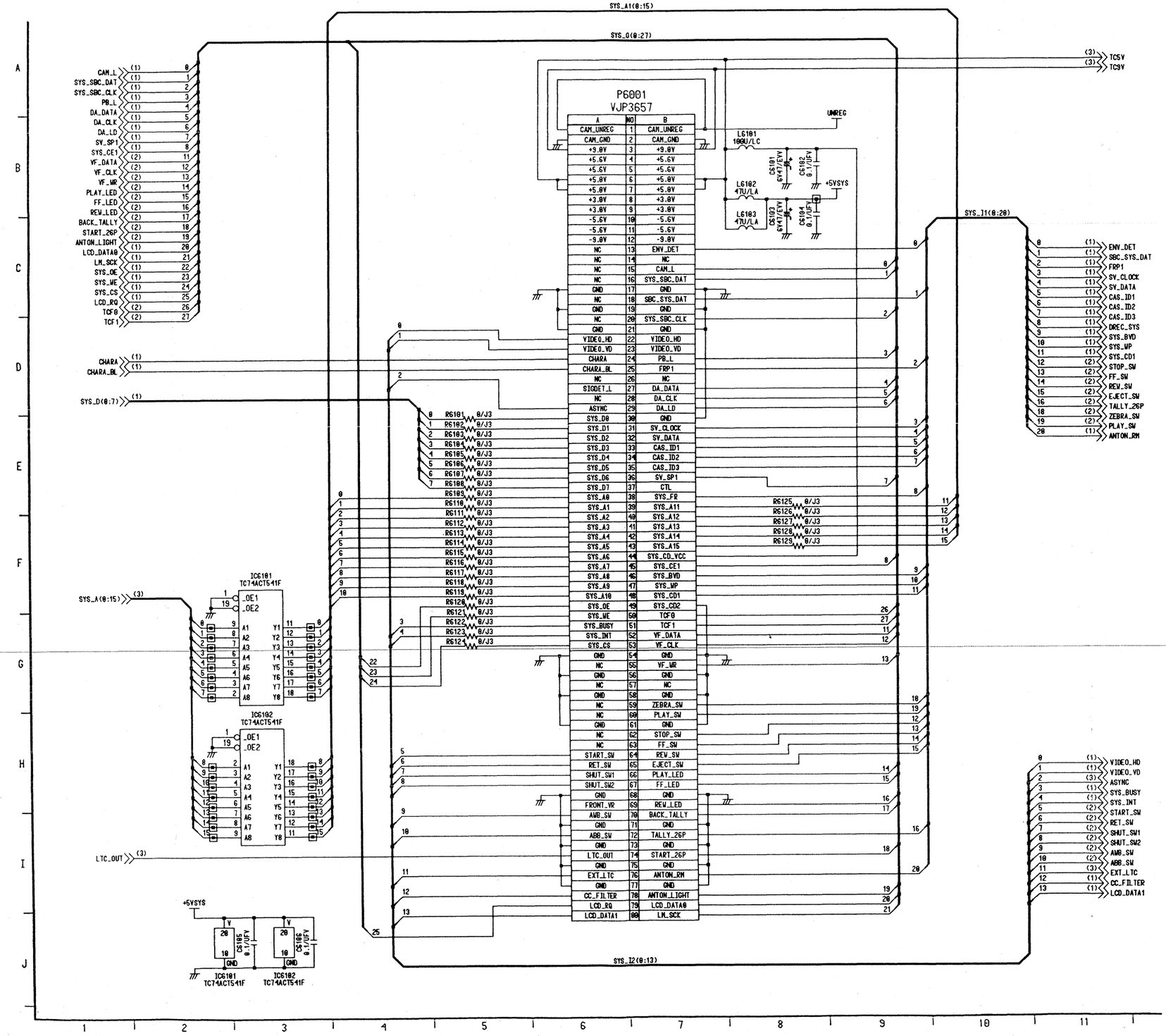


REVERSE SIDE

VTR SYSCON 2/5

2—36

VTR SYSCON (4/5) CONNECTOR SCHEMATIC DIAGRAM



2—37

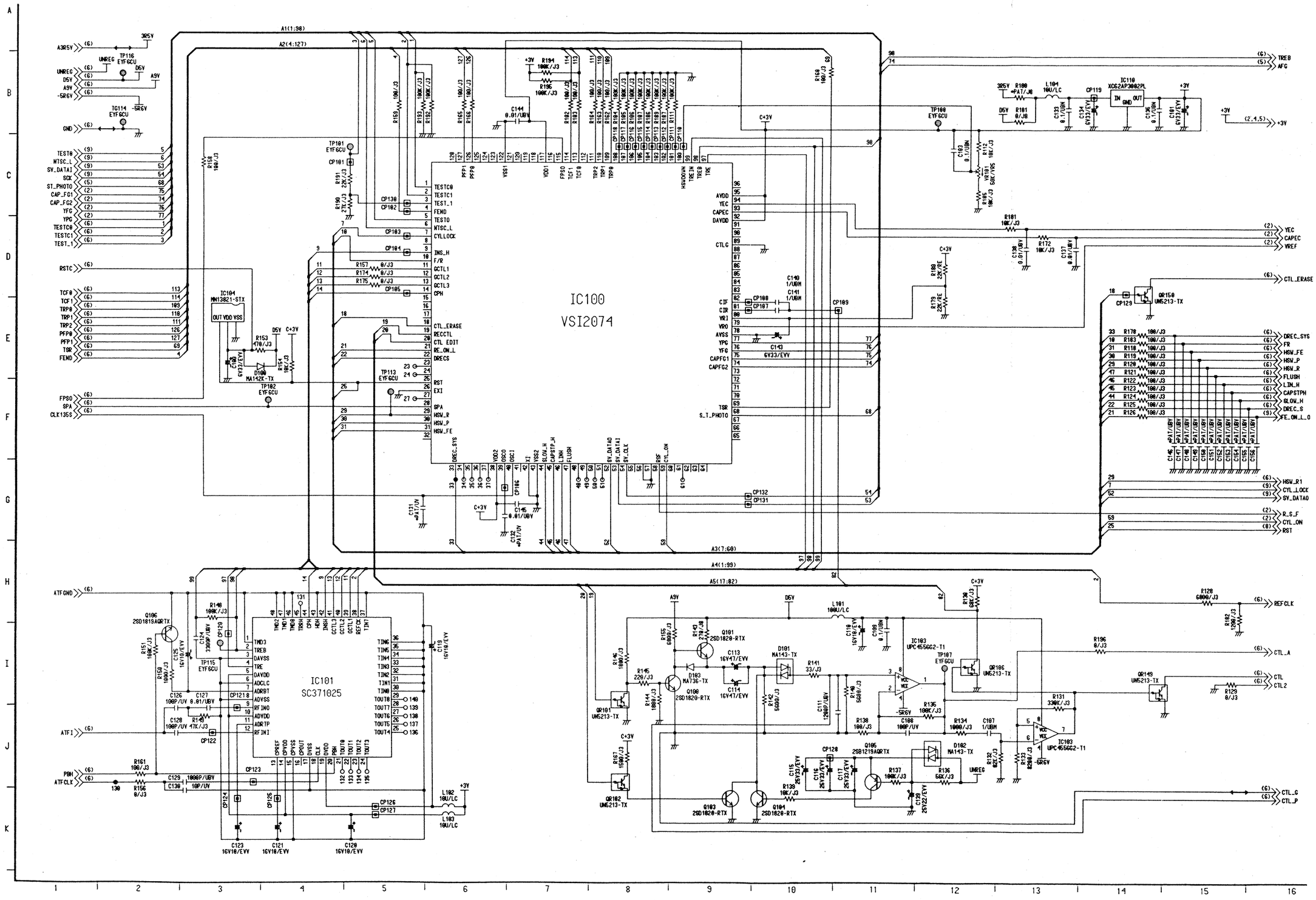
VTR SYSCON (5/5)
COMPARISON CHART BETWEEN MODELS

REF	T	P	E	ON
C6011	*PAT/UV	*PAT/UV	*PAT/UV	33P/UV
C6020	*PAT/UV	*PAT/UV	*PAT/UV	33P/UV
C6810	18P/UV	18P/UV	22P/UV	18P/UV
D6005	*PAT	*PAT	*PAT	MA728-TX
D6006	*PAT	*PAT	*PAT	MA728-TX
D6010	*PAT	*PAT	*PAT	MA728-TX
D6011	*PAT	*PAT	*PAT	MA728-TX
D6019	*PAT	*PAT	*PAT	MA728-TX
D6020	*PAT	*PAT	*PAT	MA728-TX
R6027	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R6028	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R6245	0/J3	*PAT/J3	*PAT/J3	0/J3
R6246	*PAT/J3	*PAT/J3	0/J3	0/J3
R6802	0/J3	0/J3	*PAT/J3	0/J3
R6815	*PAT/J3	*PAT/J3	*PAT/J3	100K/J3
X6802	VSX0614-T	VSX0614-T	VSX0615-T	VSX0614-T

REVERSE SIDE
VTR SYSCON 4/5

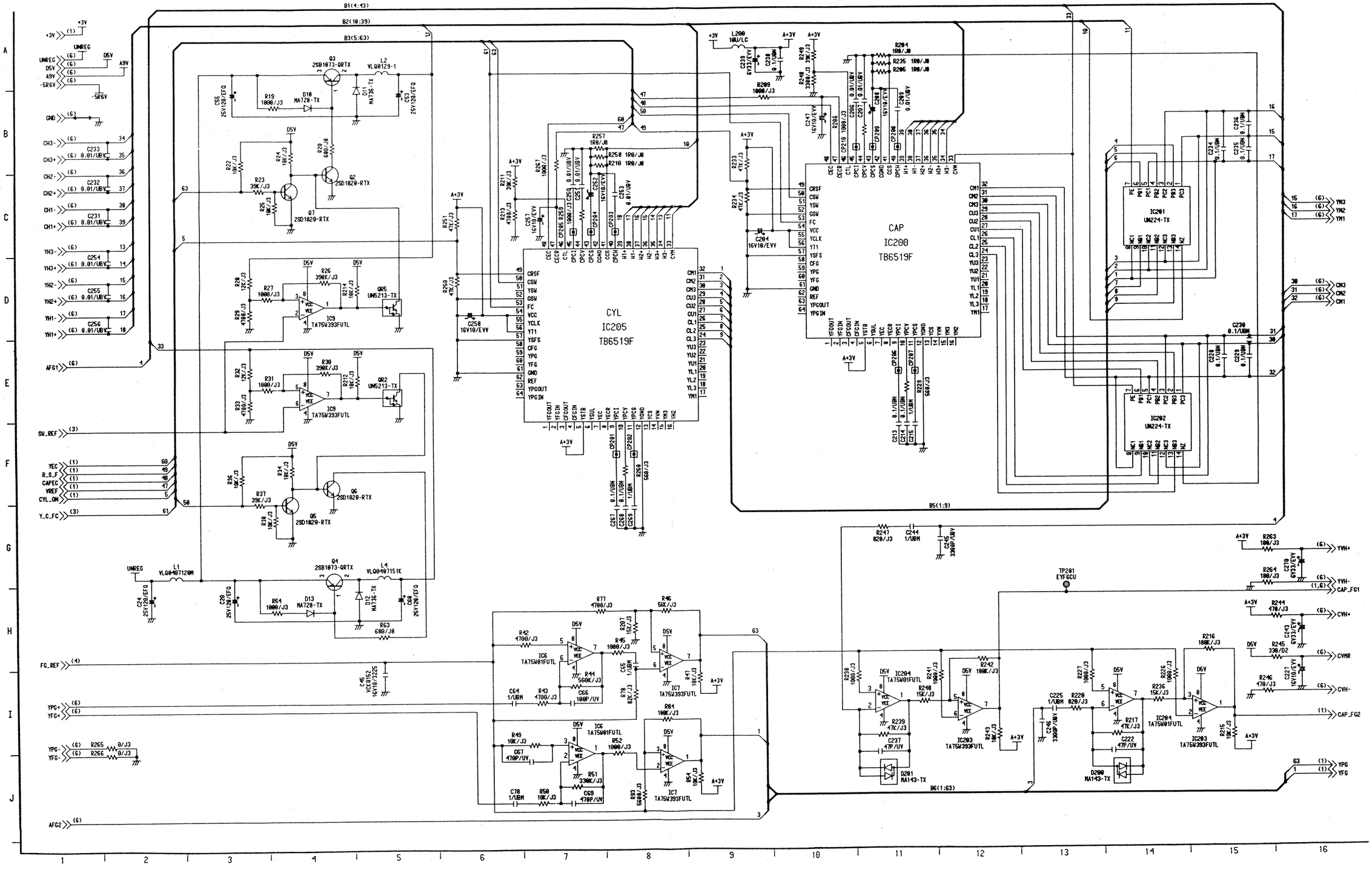
2—38

SERVO (1/9) SCHEMATIC DIAGRAM



2—39

SERVO (2/9) SCHEMATIC DIAGRAM

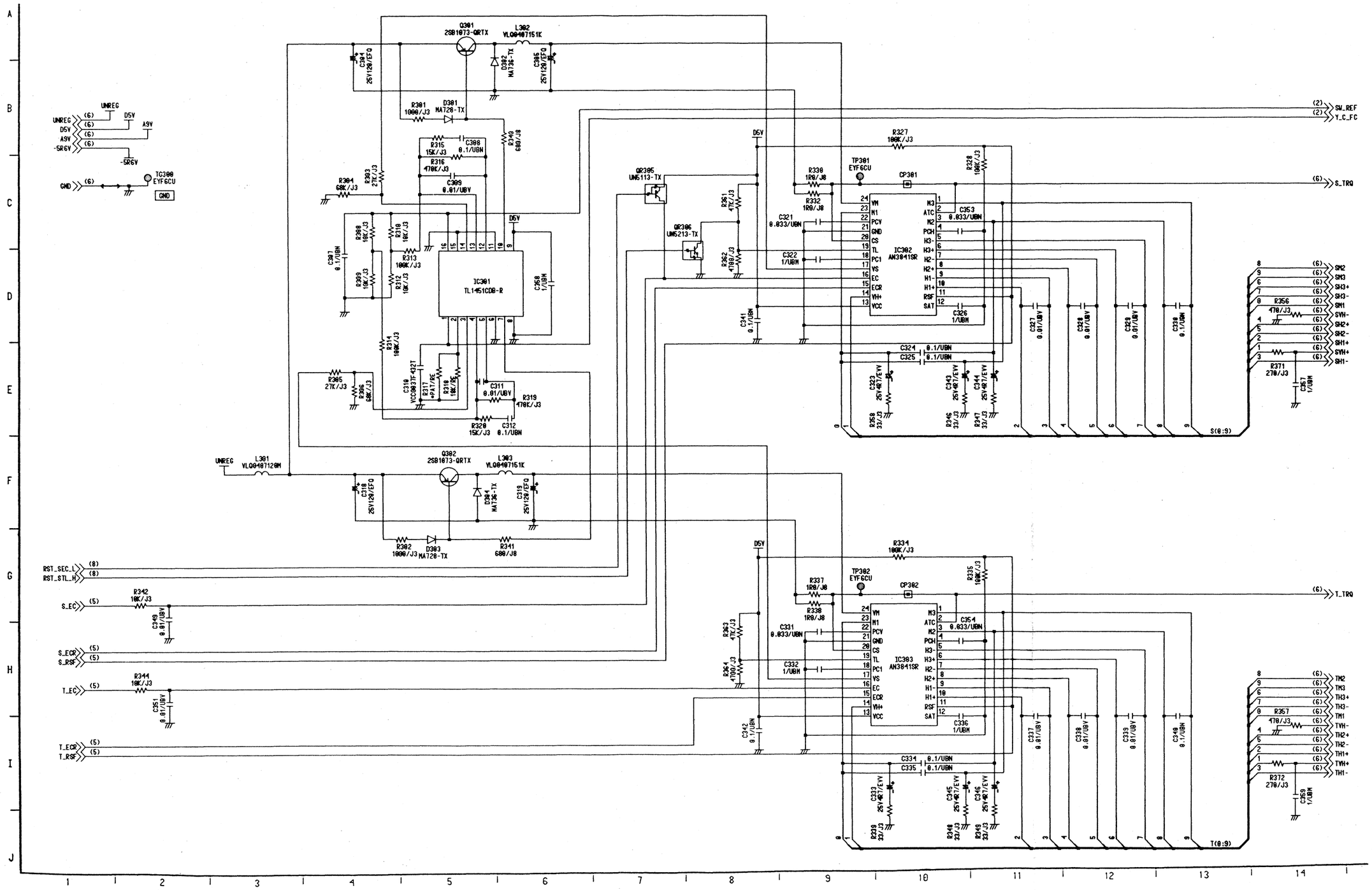


REVERSE SIDE

SERVO 1/9

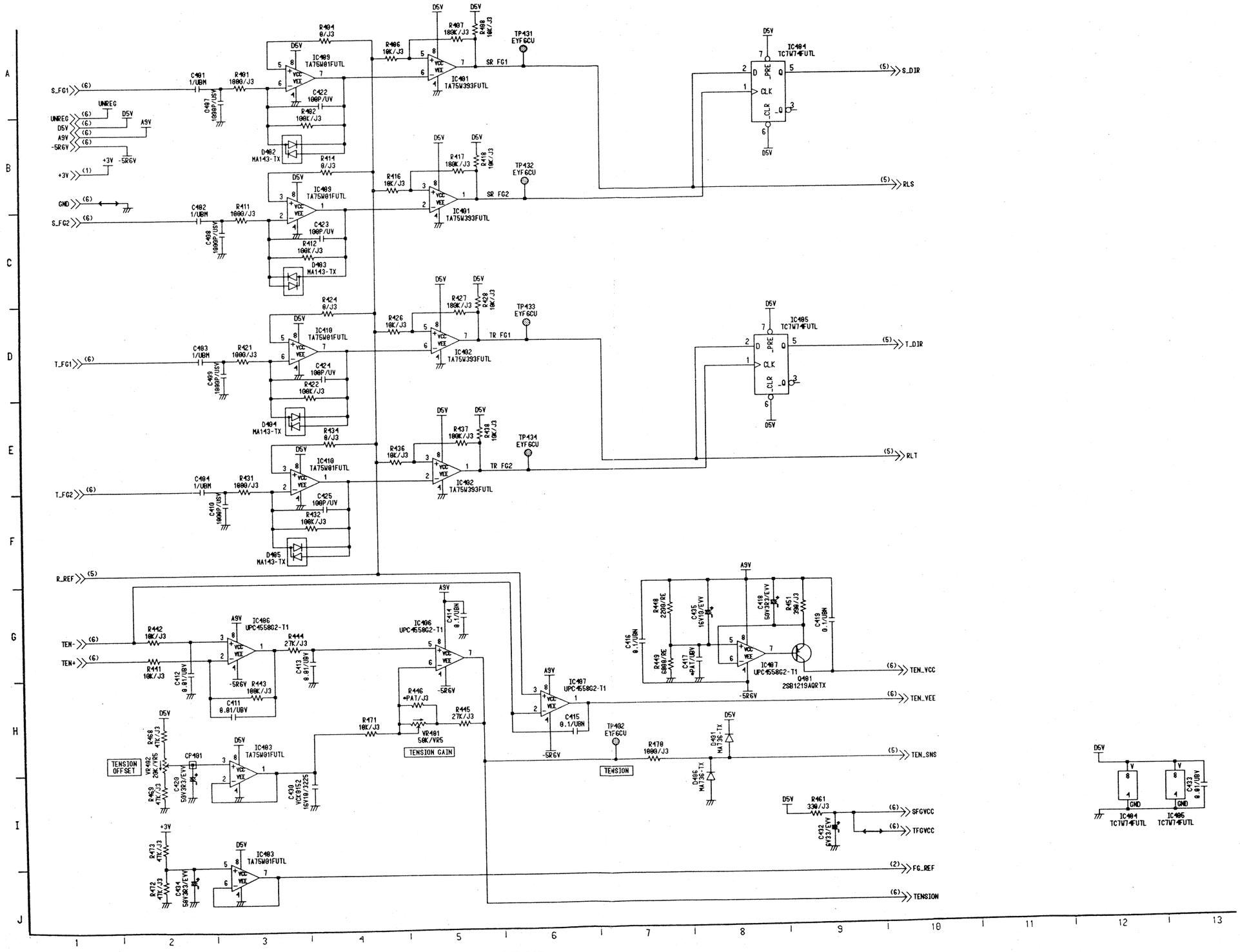
2—40

SERVO (3/9) SCHEMATIC DIAGRAM



2—41

SERVO (4/9) SCHEMATIC DIAGRAM

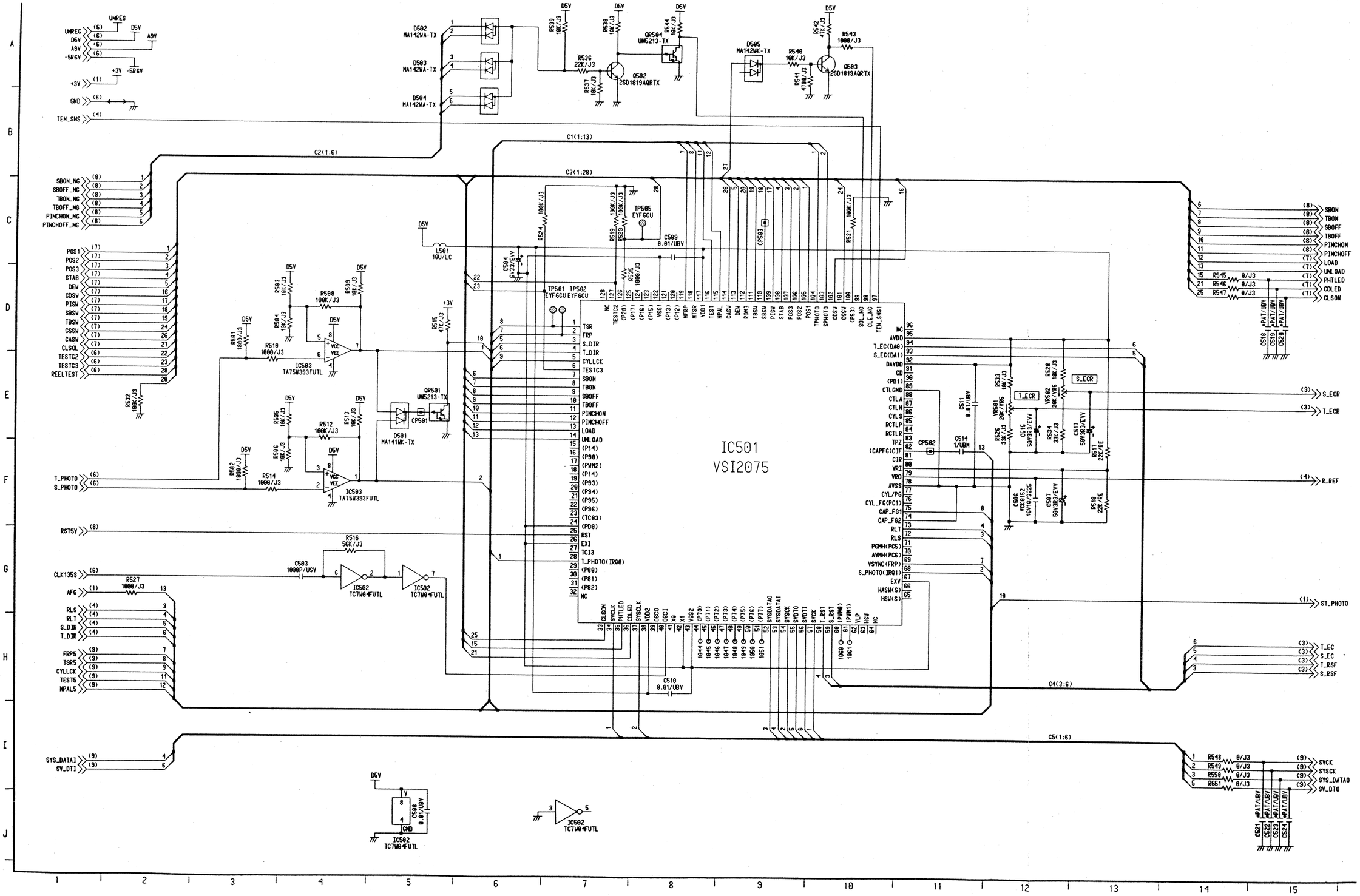


REVERSE SIDE

SERVO 3/9

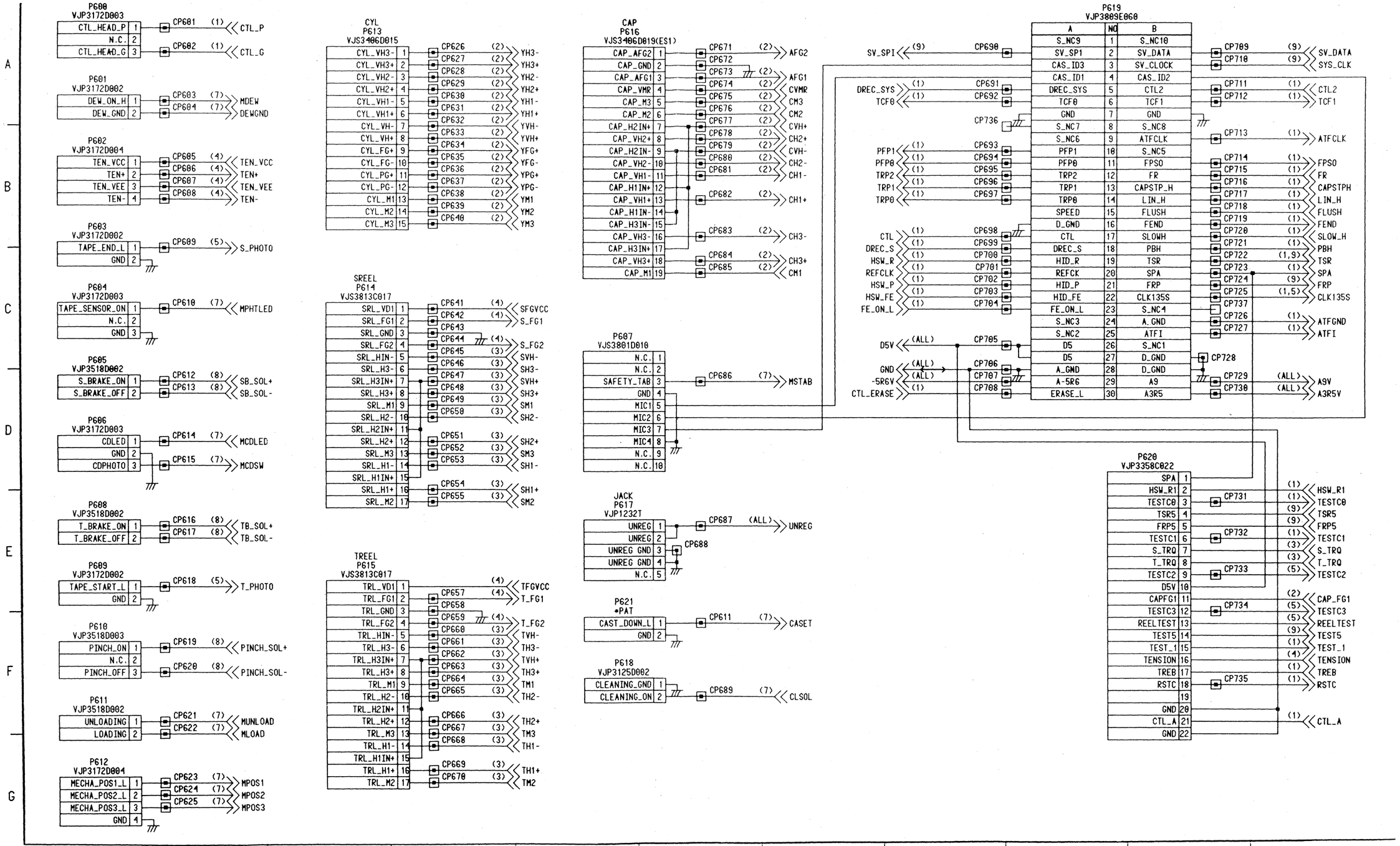
2—42

SERVO (5/9) SCHEMATIC DIAGRAM



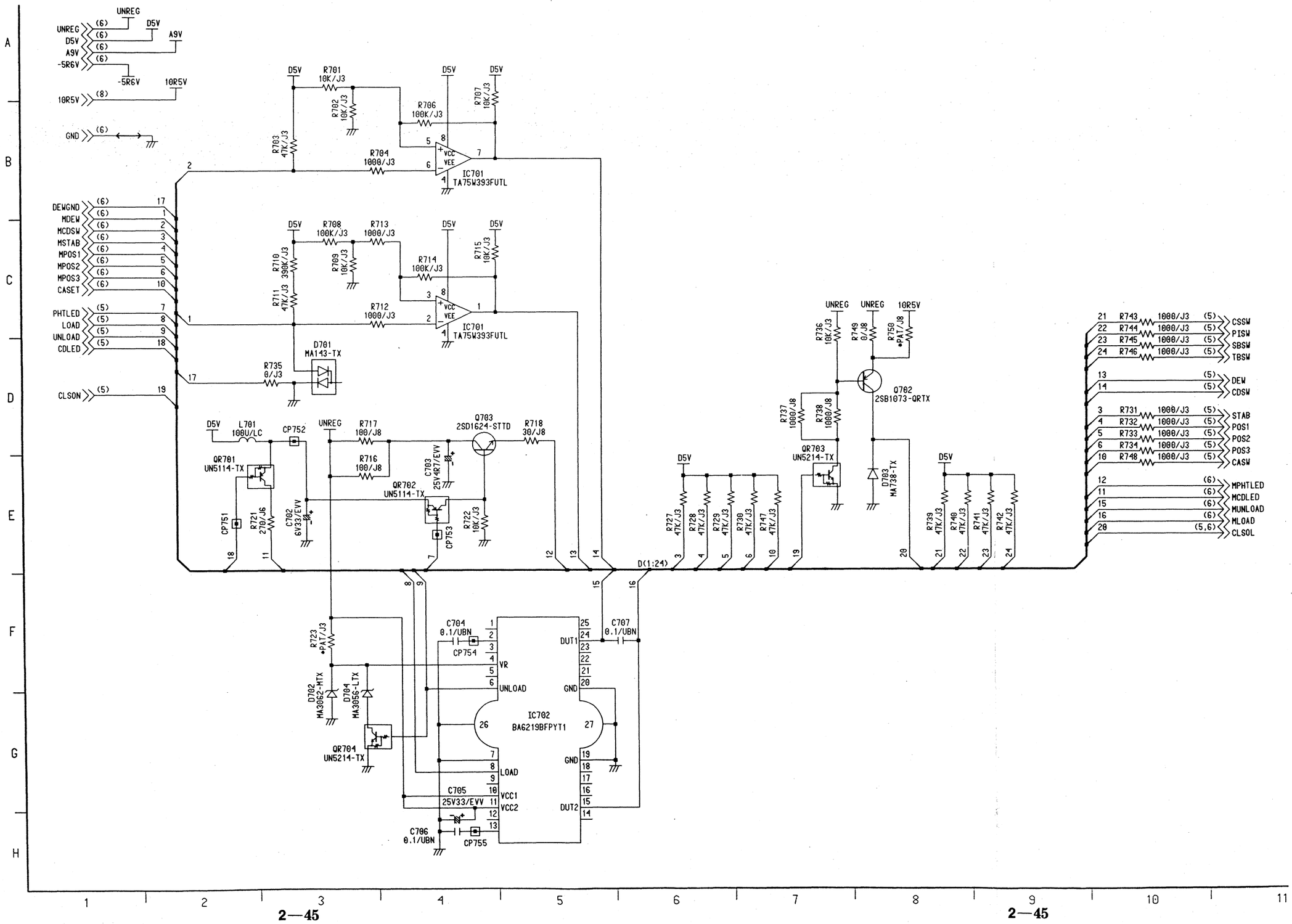
2—43

SERVO (6/9) SCHEMATIC DIAGRAM



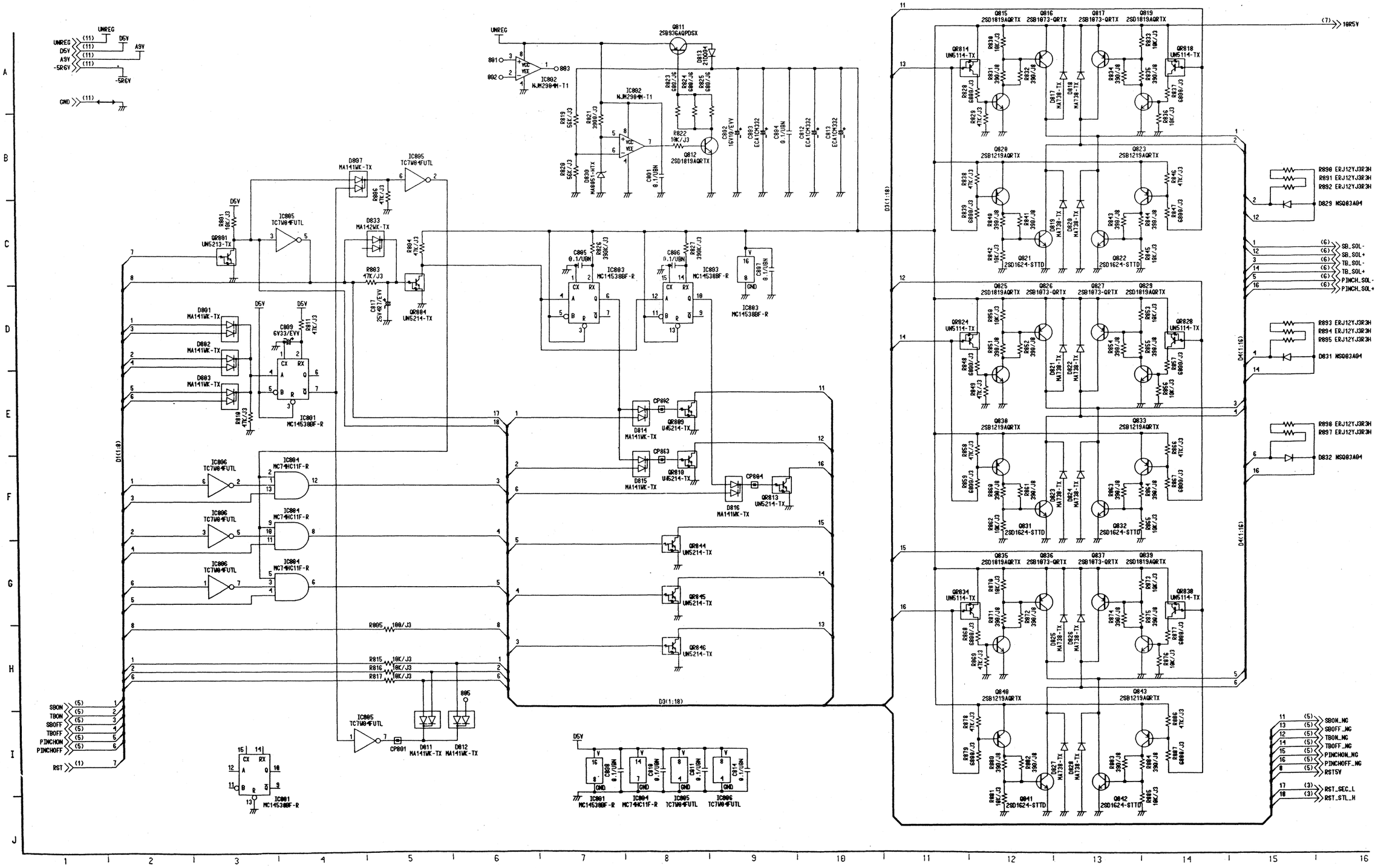
REVERSE SIDE

SERVO (7/9) SCHEMATIC DIAGRAM



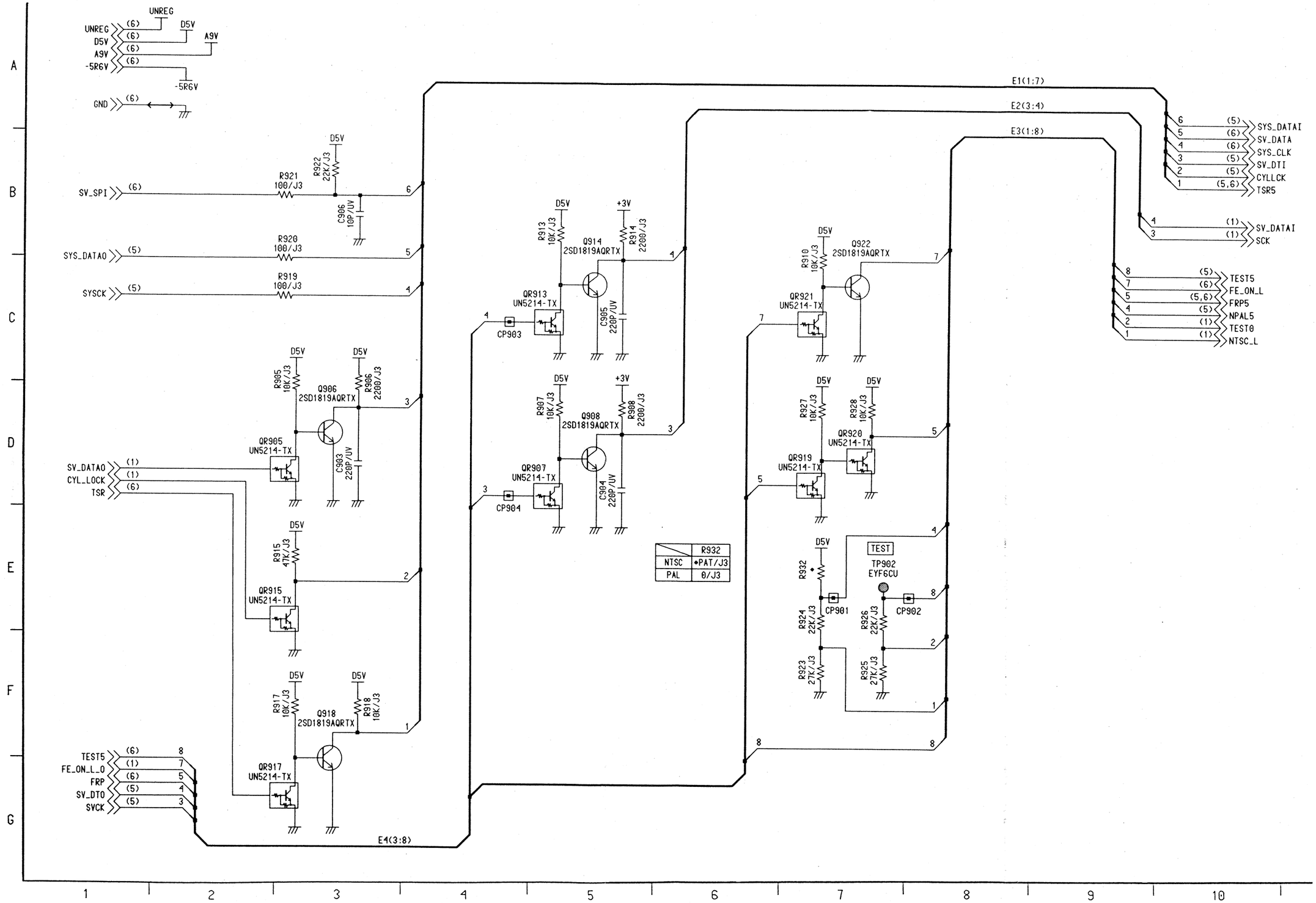
2—45

SERVO (8/9) SCHEMATIC DIAGRAM



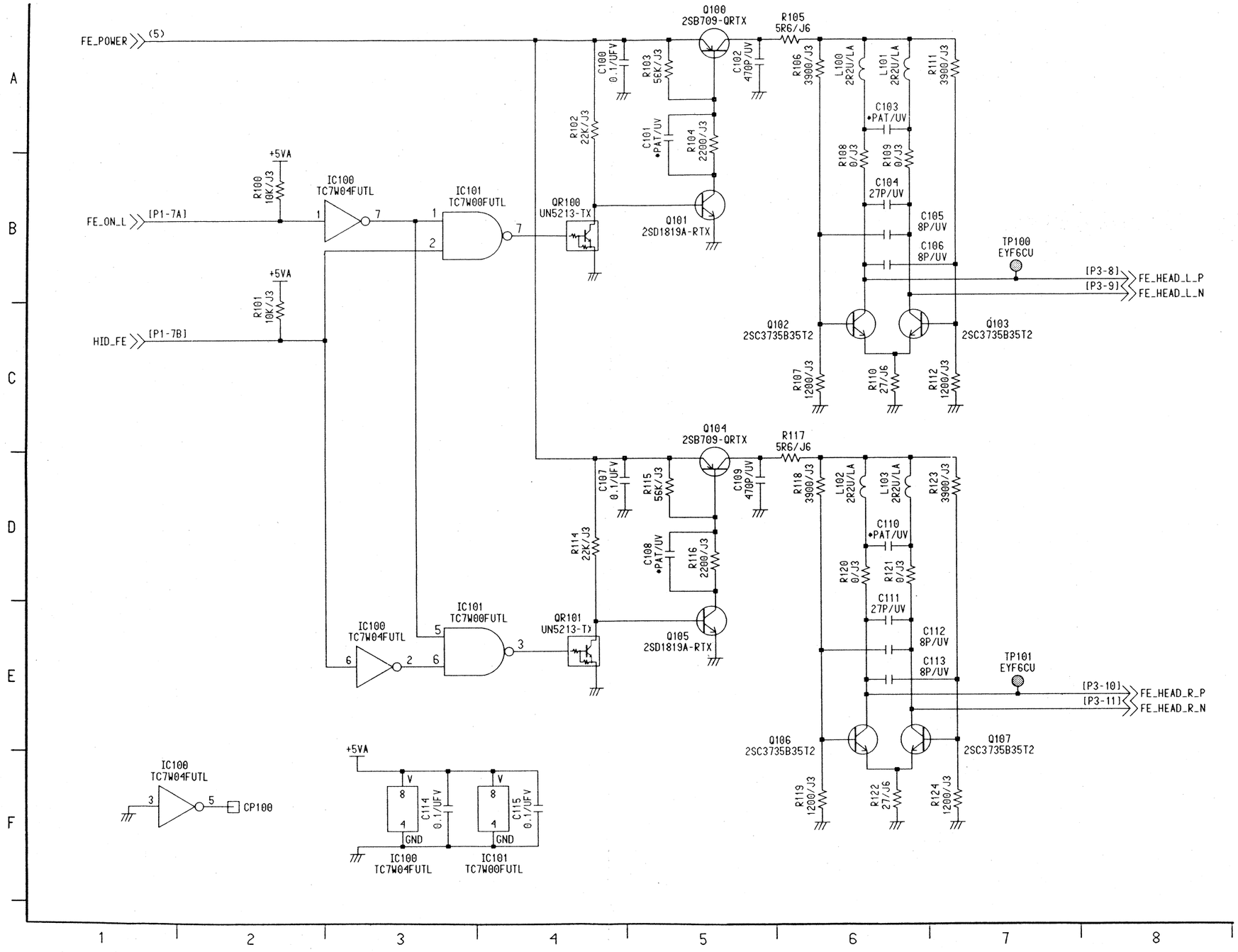
REVERSE SIDE

SERVO (9/9) SCHEMATIC DIAGRAM



2—47

RF (1/5) SCHEMATIC DIAGRAM

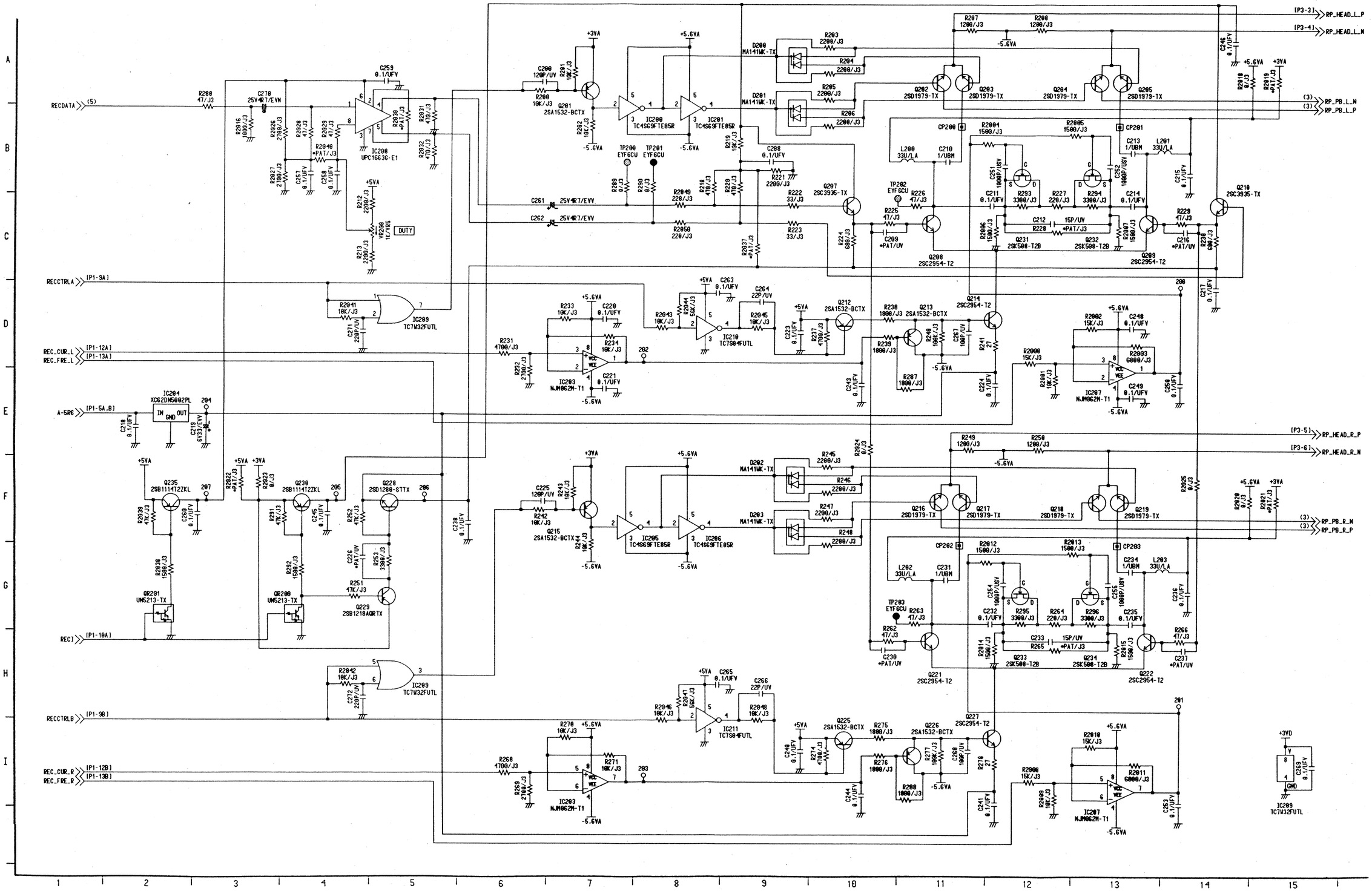


REVERSE SIDE

SERVO 9/9

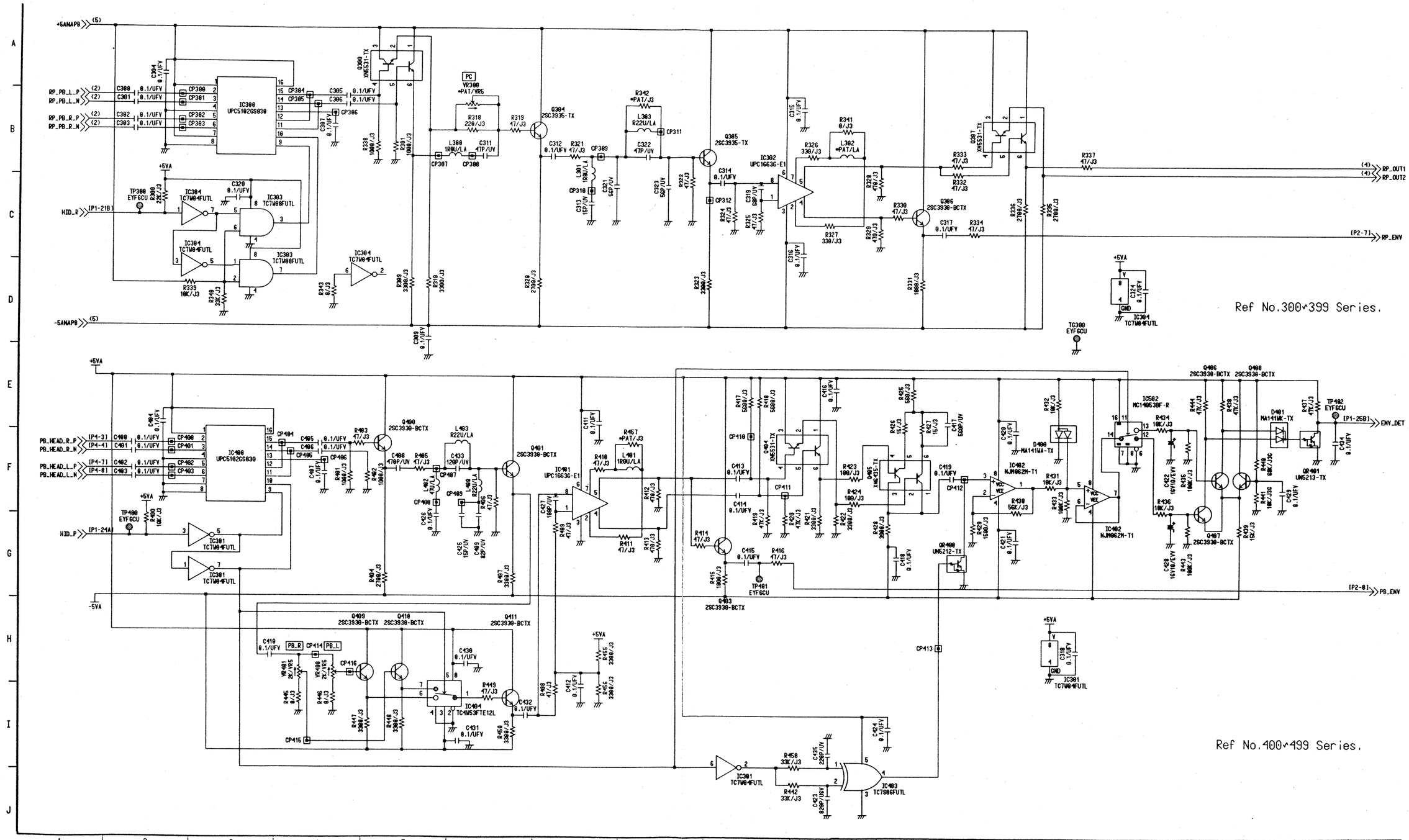
2—48

RF (2/5) SCHEMATIC DIAGRAM



2—49

RF (3/5) SCHEMATIC DIAGRAM

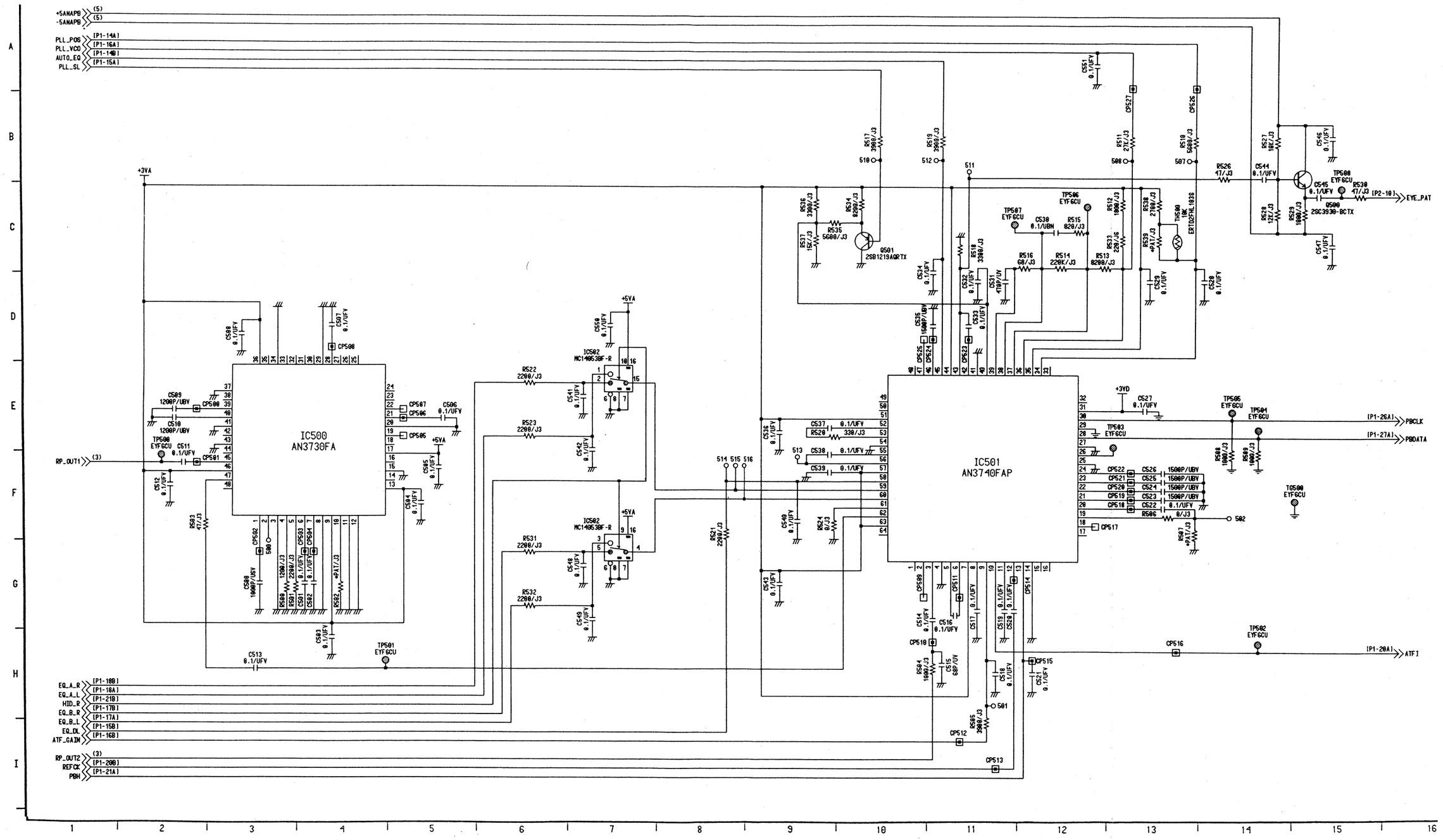


REVERSE SIDE

RF 2/5

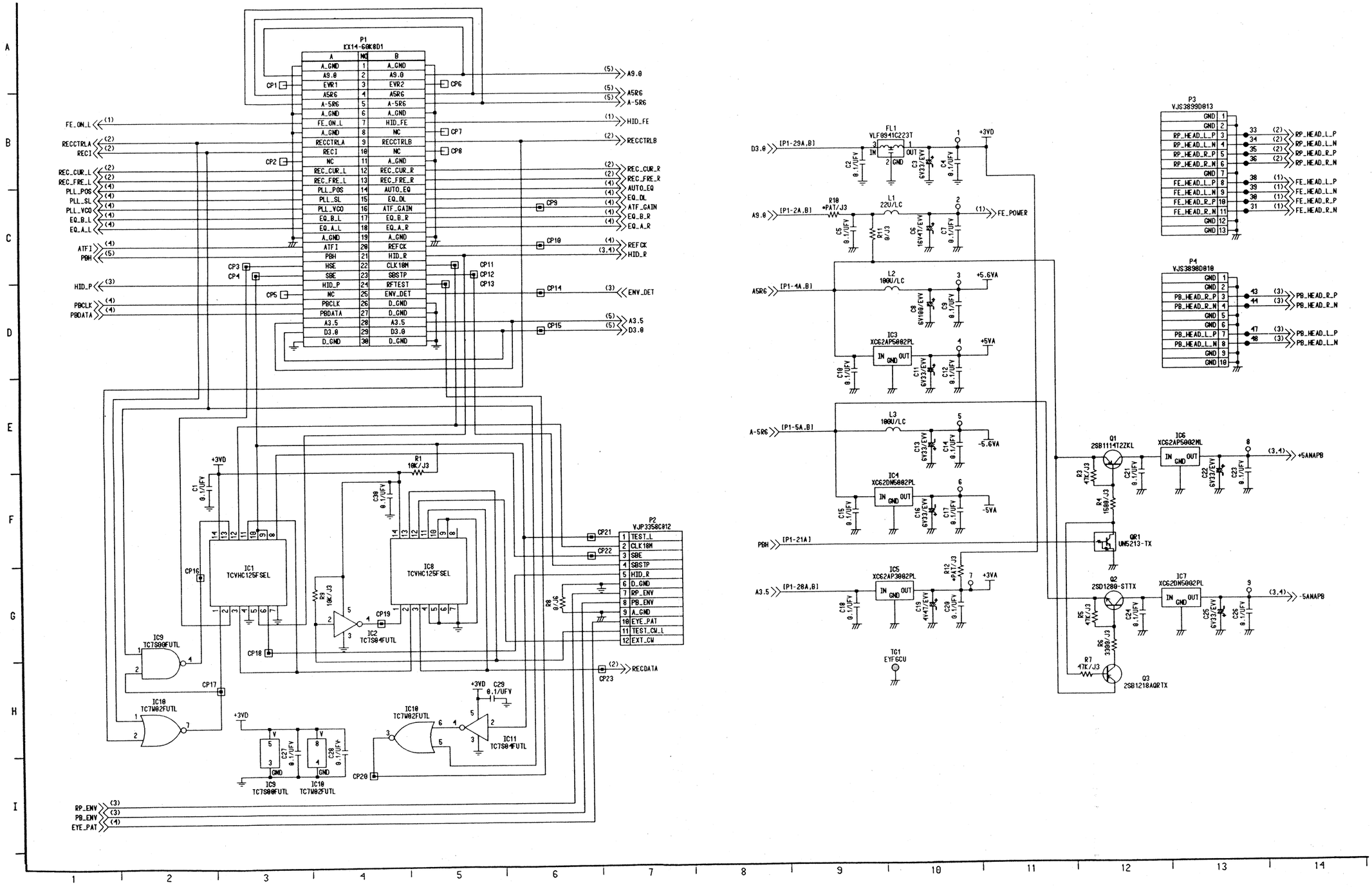
2—50

RF (4/5) SCHEMATIC DIAGRAM



2—51

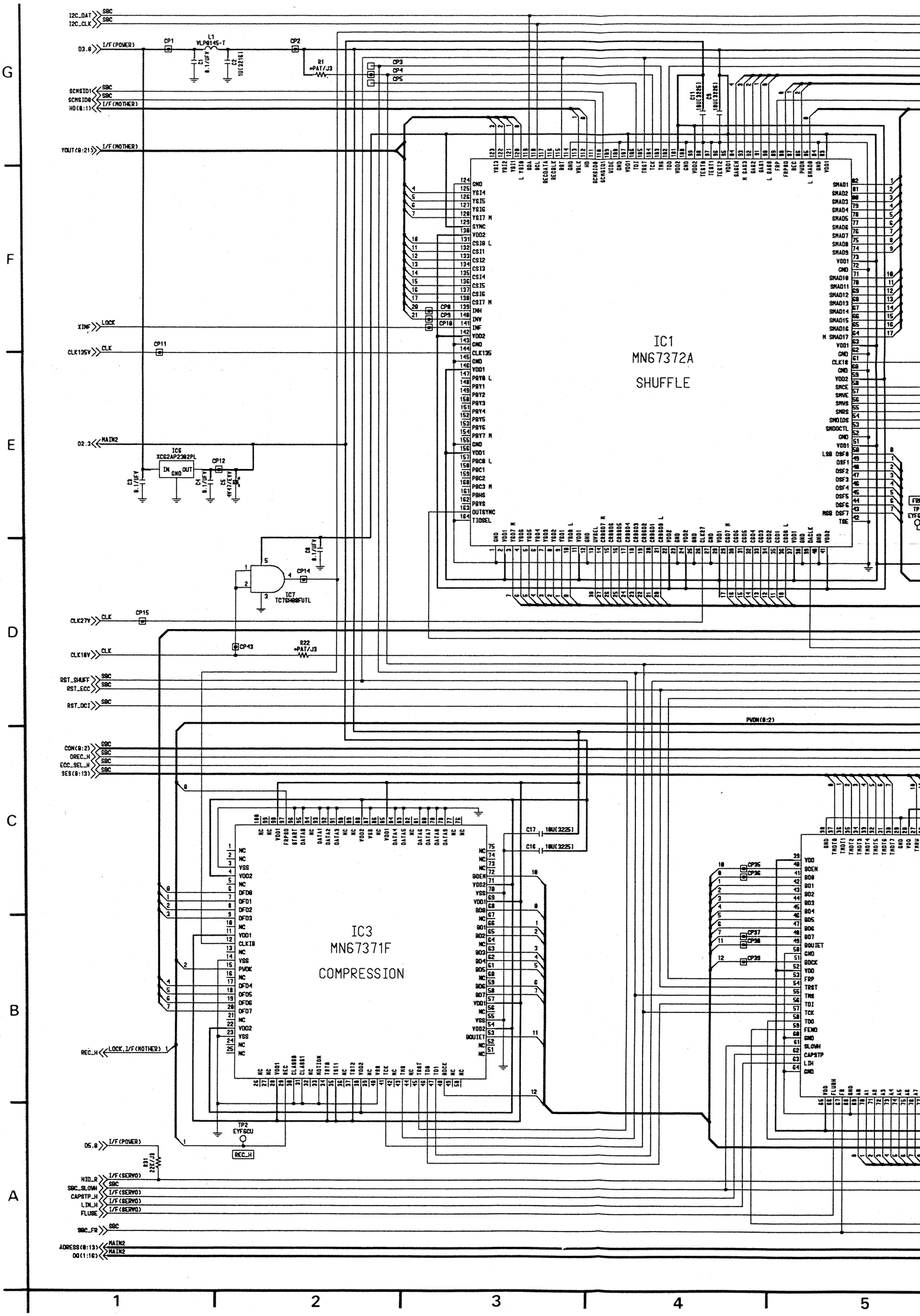
RF (5/5) SCHEMATIC DIAGRAM

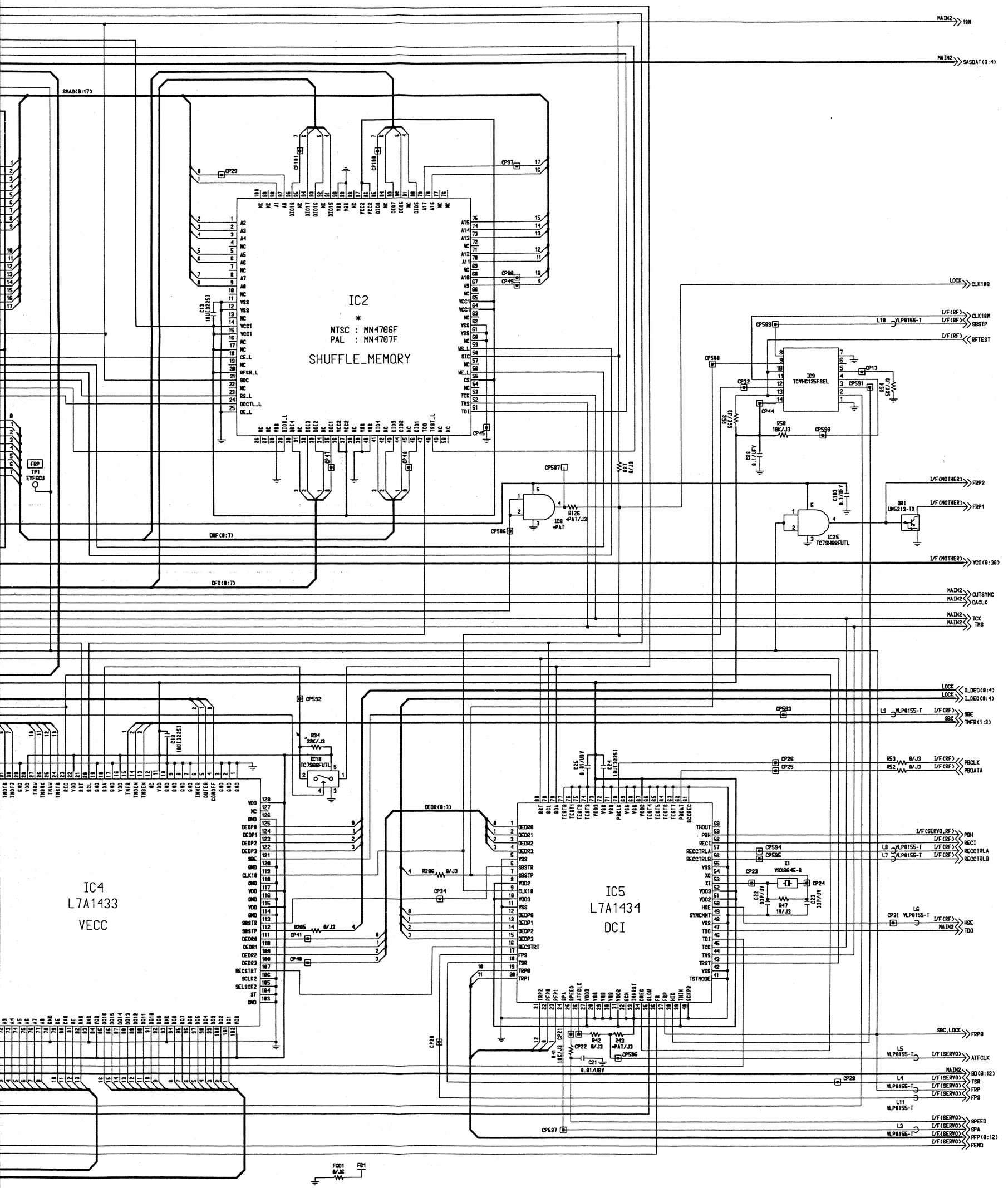


REVERSE SIDE

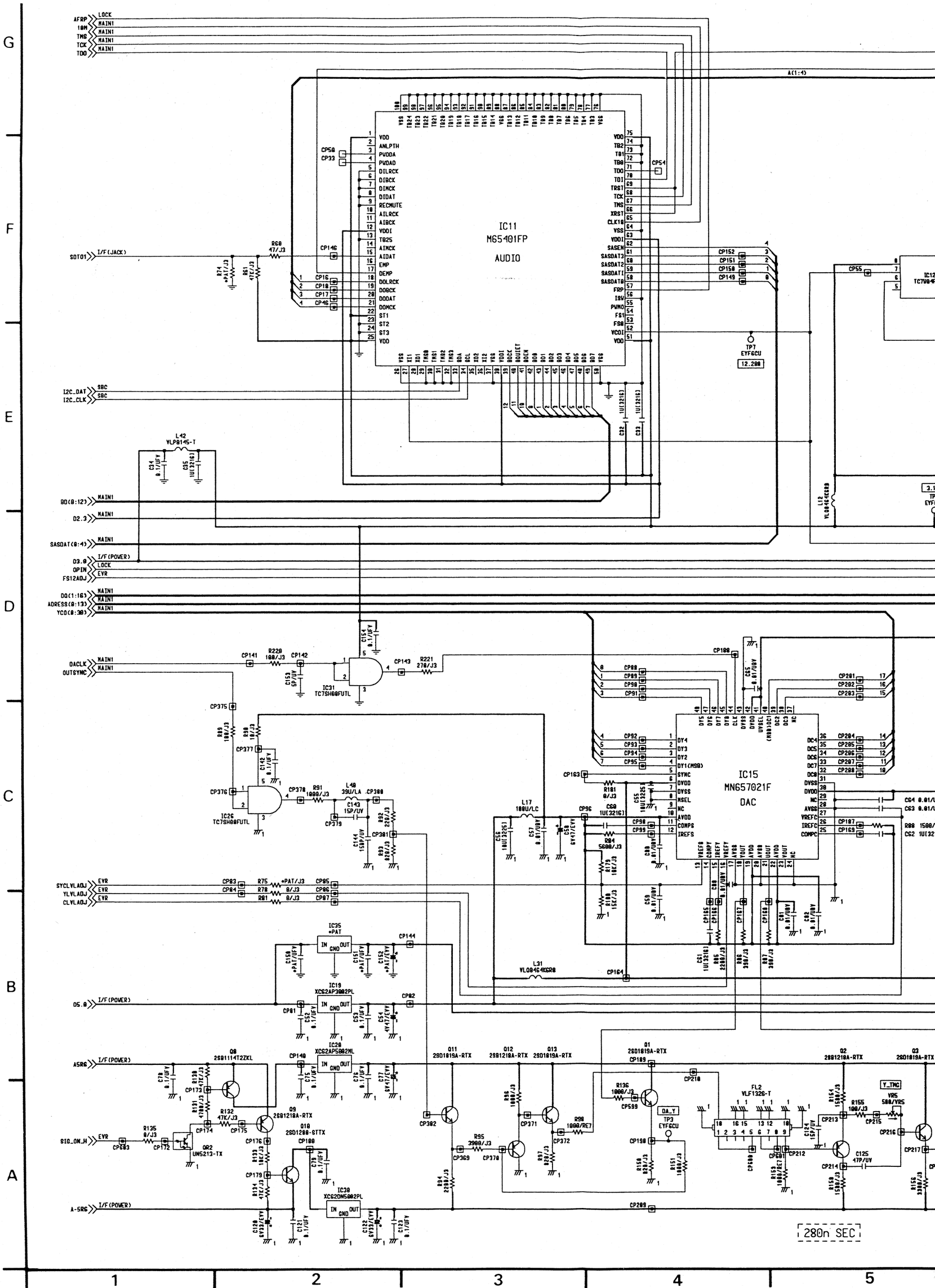
RF 4/5

VIDEO MAIN (1/7) MAIN 1 SCHEMATIC DIAGRAM




IC2
*
NTSC : MN4706F
PAL : MN4707F
SHUFFLE_MEMORY
IC4
L7A1433
VECC
IC5
L7A1434
DCI
IC9
TC7WHC125F9EL
IC25
TC7SH08FUTL
IC18
TC7S66FUTL
IC8
*PAT
IC6
*PAT
SMAD(8:17)
DBF(8:7)
DFD(8:7)
DEDR(8:3)
MAIN2 10M
MAIN2 SASDAT(0:4)
LOCK CLK108
I/F(RF) CLK10M
I/F(RF) 888TP
I/F(RF) RFTEST
L10 VLP0155-T
I/F(MOTHER) FRP2
I/F(MOTHER) FRP1
I/F(MOTHER) YCO(0:39)
QR1 UN5213-TX
MAIN2 OUTSYNC
MAIN2 DACLK
MAIN2 TCK
MAIN2 TMS
LOCK Q_DEO(0:4)
LOCK I_DEO(0:4)
L9 VLP0155-T I/F(RF) SBC
SBC TMFR(1:3)
R53 0/J3 I/F(RF) PBCLK
R52 0/J3 I/F(RF) PBDATA
I/F(SERVO,RF) PBH
I/F(RF) RECI
L8 VLP0155-T I/F(RF) RECCTRLA
L7 VLP0155-T I/F(RF) RECCTRLB
L6 CP31 VLP0155-T I/F(RF) HSE
MAIN2 TDO
SBC,LOCK FRP0
L5 VLP0155-T I/F(SERVO) ATFCLK
MAIN2 BD(0:12)
L4 VLP0155-T I/F(SERVO) TSR
I/F(SERVO) FRP
I/F(SERVO) FPS
L11 VLP0155-T
L3 VLP0155-T I/F(SERVO) SPEED
I/F(SERVO) SPA
I/F(SERVO) PFP(0:12)
I/F(SERVO) FEMD
R24 22K/J3
R206 0/J3
R205 0/J3
R207 0/J3
R42 0/J3
R43 *PAT/J3
R126 *PAT/J3
R50 10K/J3
R47 1M/J3
R54 56K/J3
R56 56K/J3
R27 0/J3
C19 10U/25V
C24 10U/25V
C25 0.01/50V
C21 0.01/50V
C26 0.1/10FV
C103 0.1/10FV
C22 33P/50V
C23 33P/50V
X1 YSX964S-B
CP29
CP97
CP98
CP99
CP45
CP46
CP47
CP48
CP41
CP40
CP34
CP28
CP32
CP44
CP13
CP591
CP588
CP589
CP590
CP587
CP586
CP592
CP593
CP26
CP25
CP594
CP595
CP23
CP24
CP31
CP22
CP21
CP27
CP596
CP597
FRP TP1 EYFGCU
FGD1 0/J3
FG1

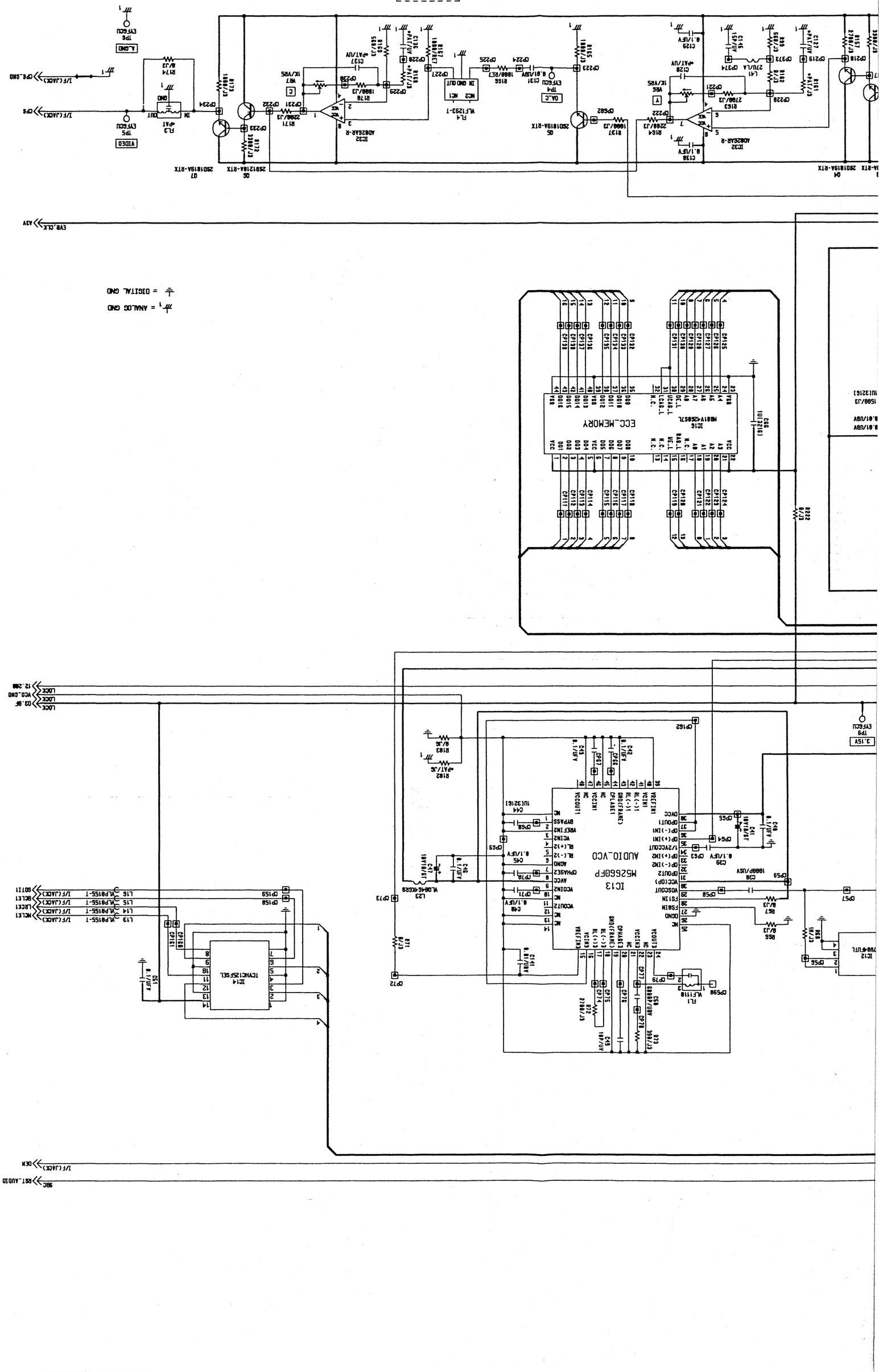
VIDEO MAIN (2/7) MAIN 2 SCHEMATIC DIAGRAM



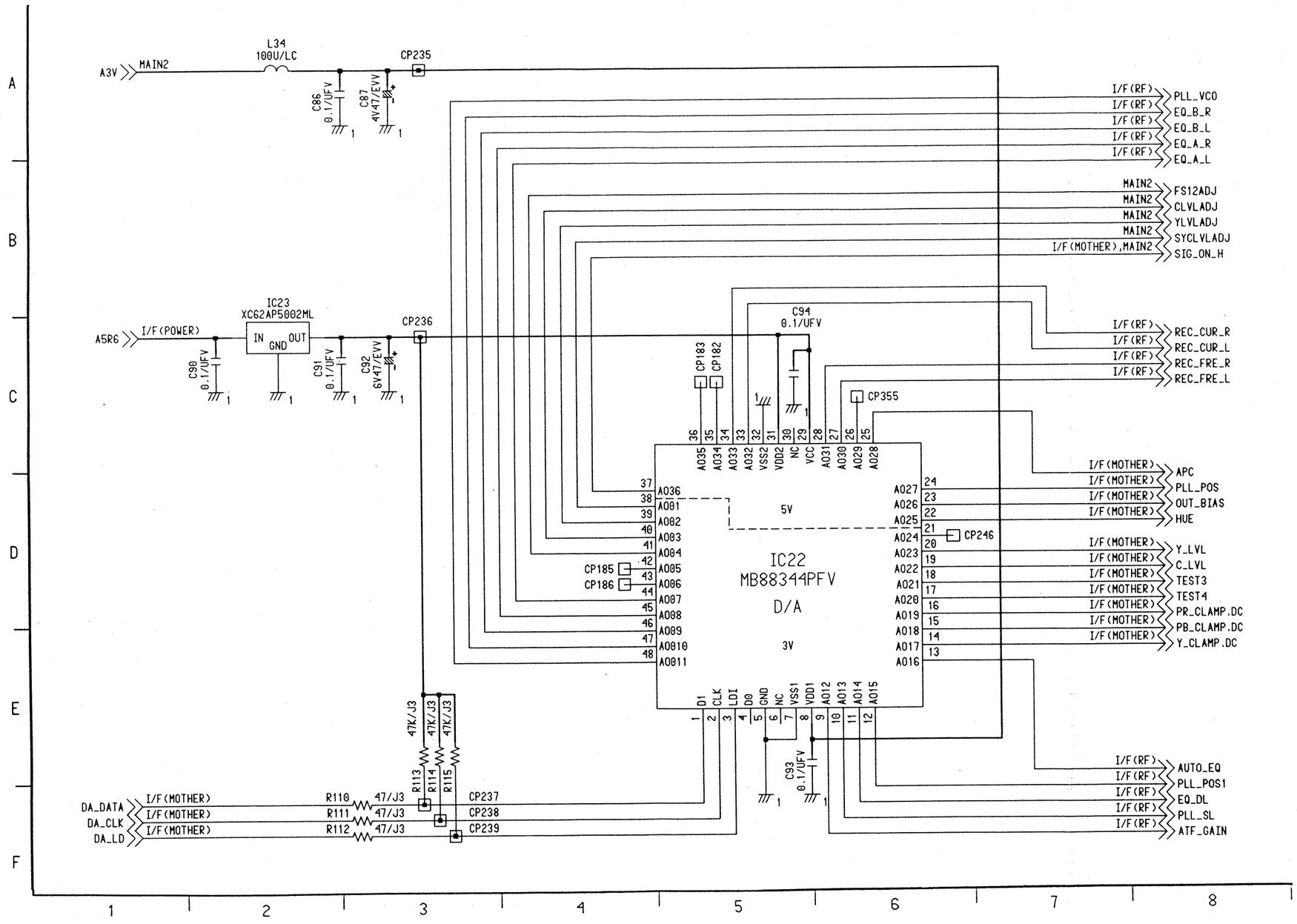
180n SEC

= ANALOG GND

= DIGITAL GND

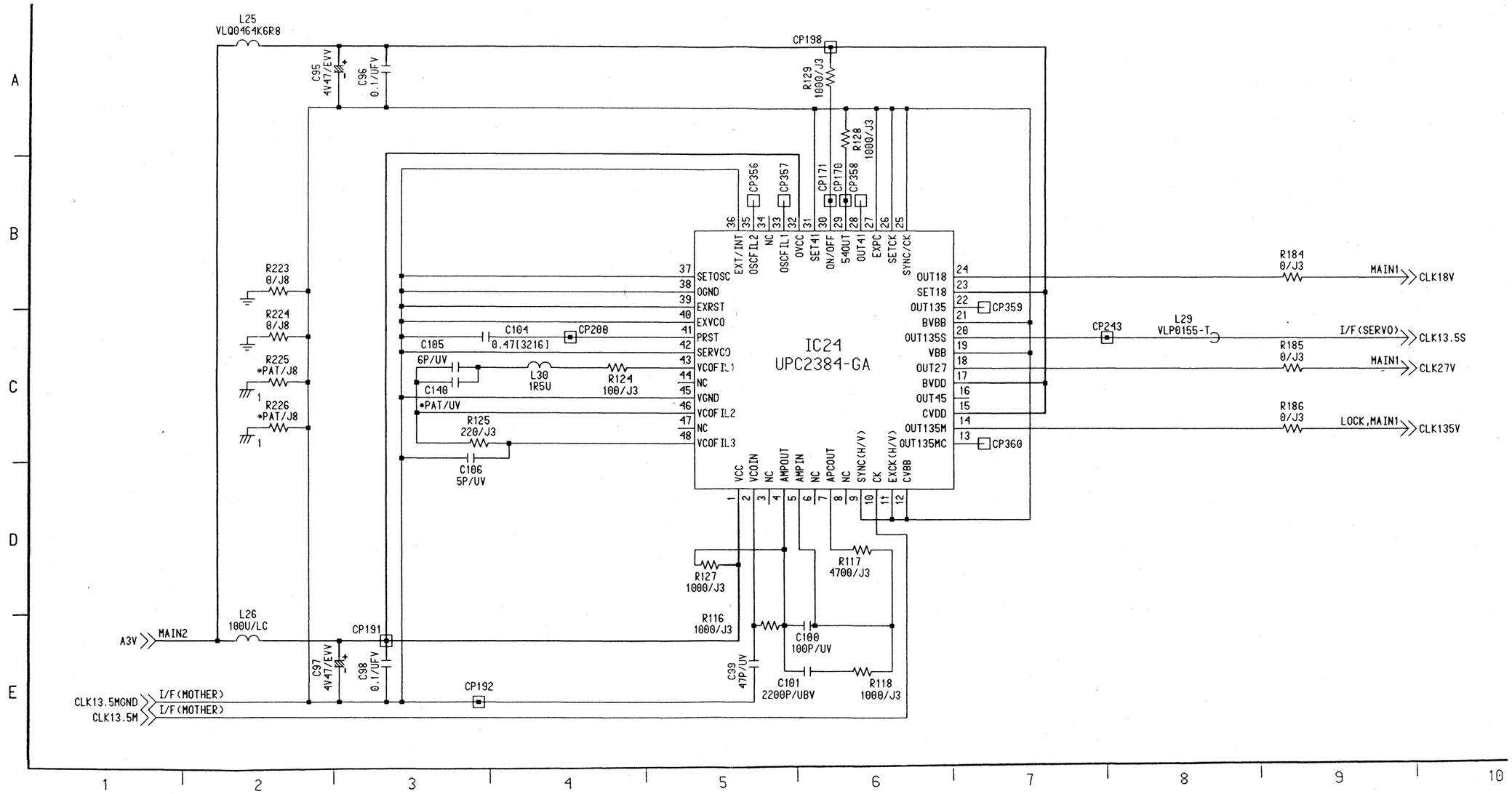


VIDEO MAIN (3/7) EVR SCHEMATIC DIAGRAM



2—55

VIDEO MAIN (4/7) SYNC CLK SCHEMATIC DIAGRAM

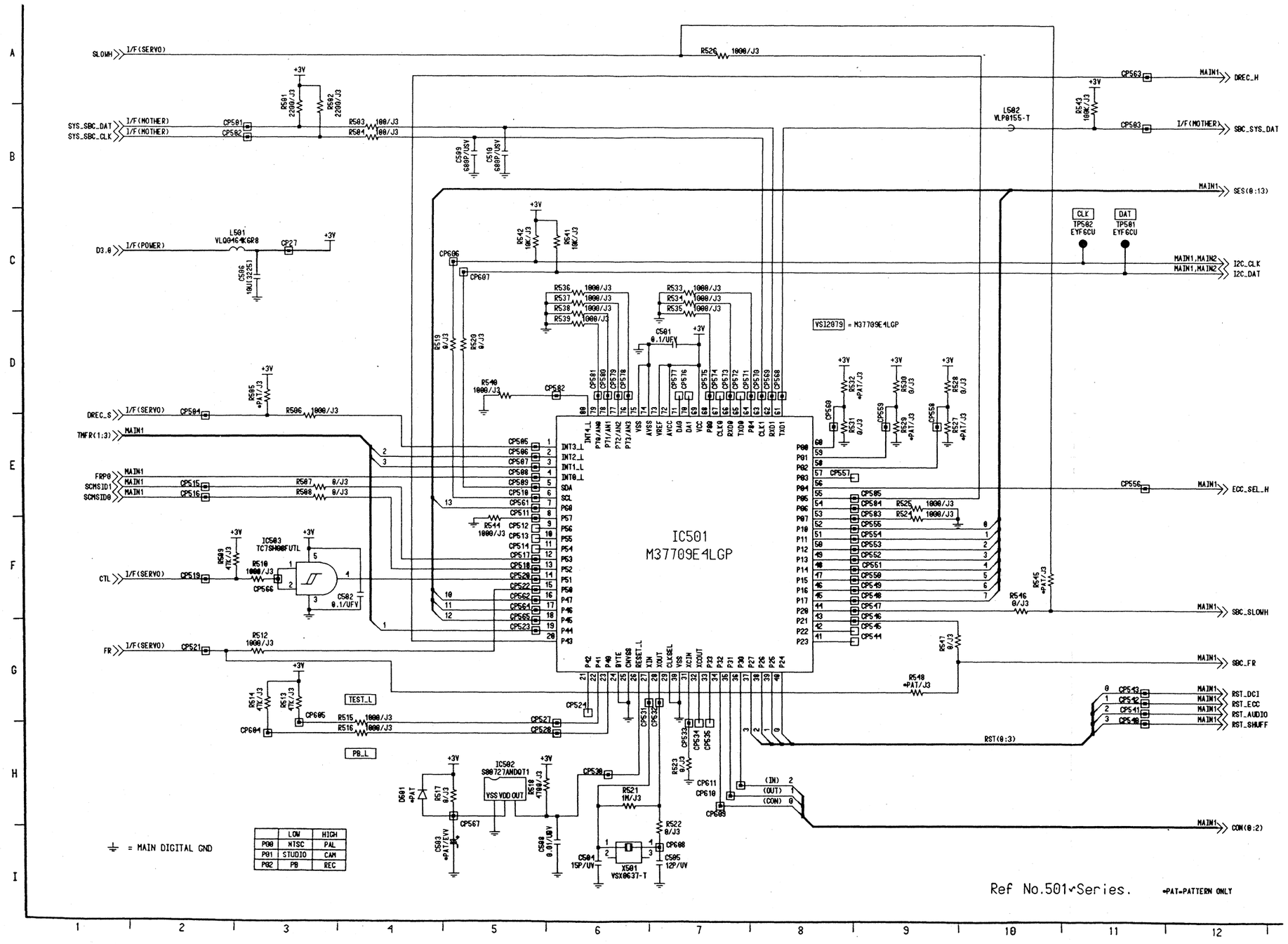


REVERSE SIDE

VIDEO MAIN 3/7

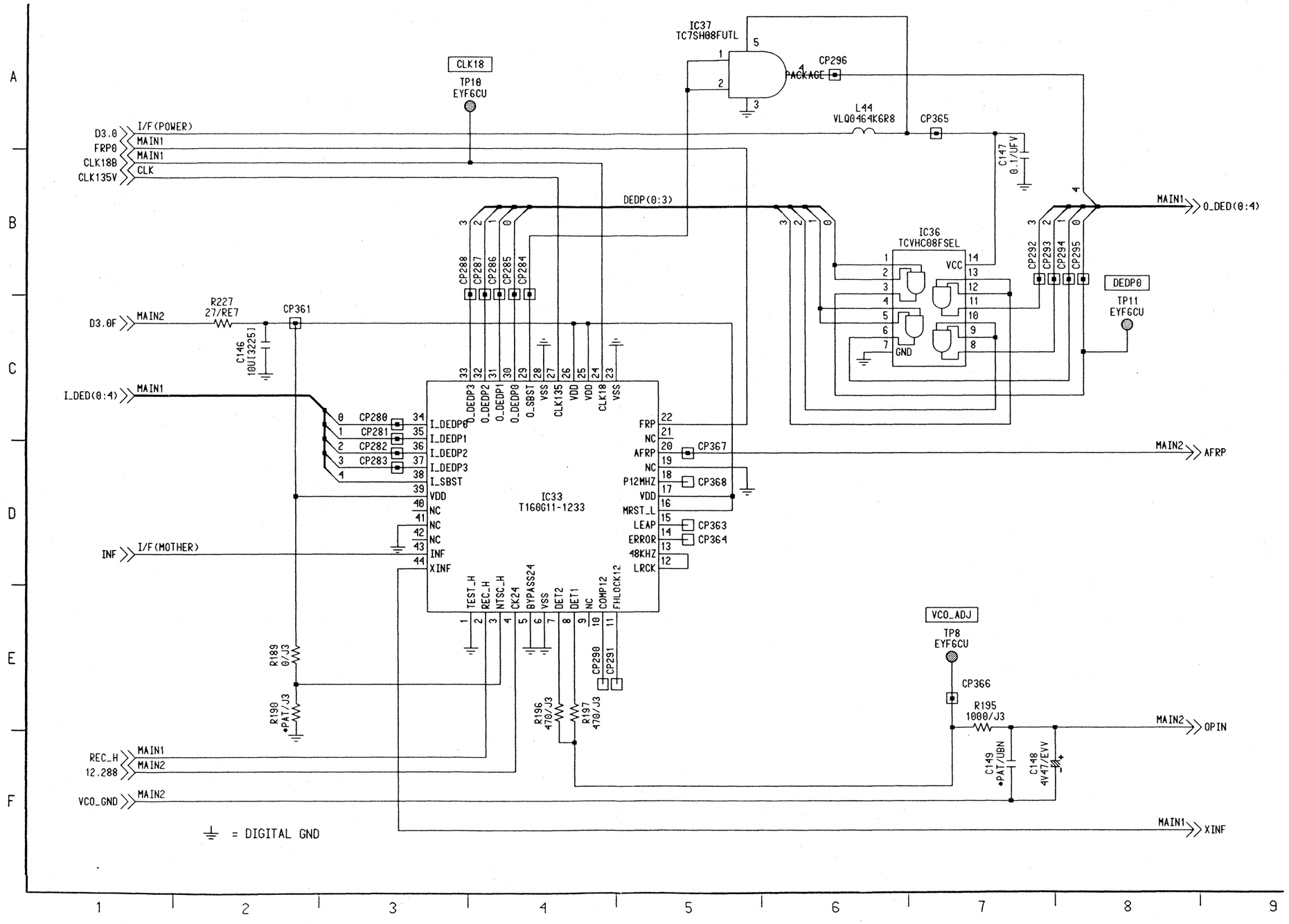
2—56

VIDEO MAIN (5/7) SBC SCHEMATIC DIAGRAM



2—57

VIDEO MAIN (6/7) LOCK SCHEMATIC DIAGRAM

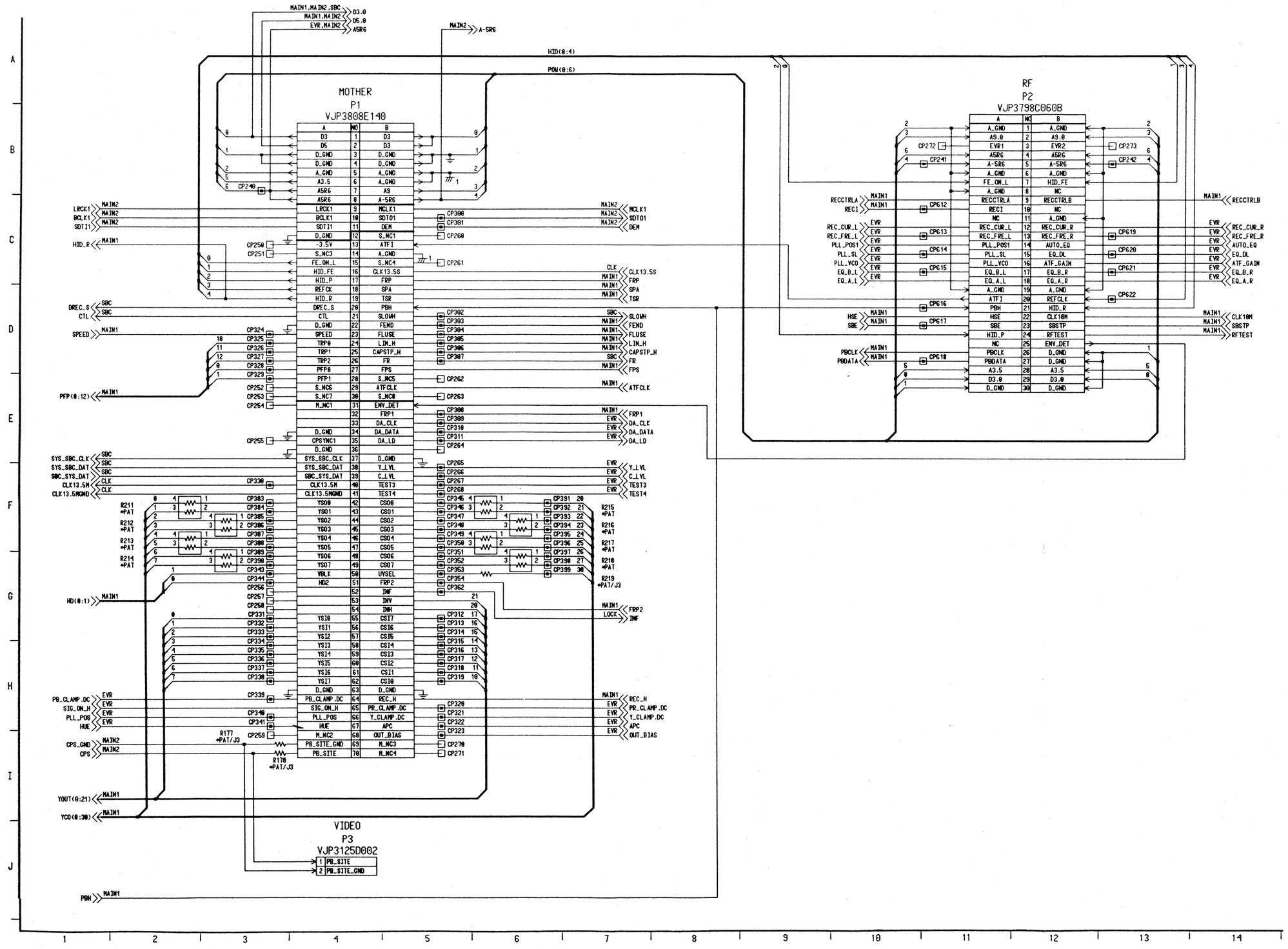


REVERSE SIDE

VIDEO MAIN 5/7

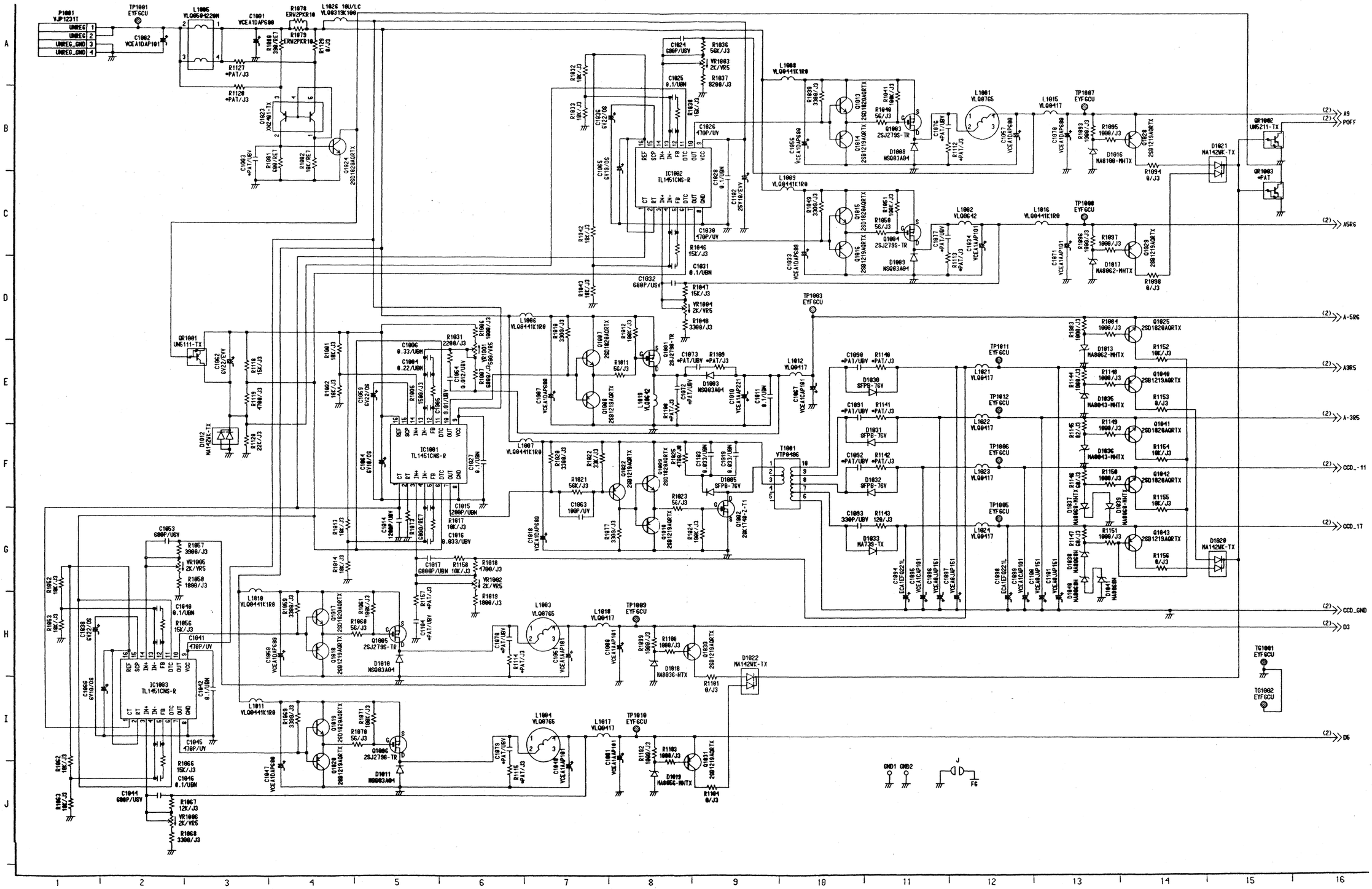
2—58

VIDEO MAIN (7/7) I/F SCHEMATIC DIAGRAM



2—59

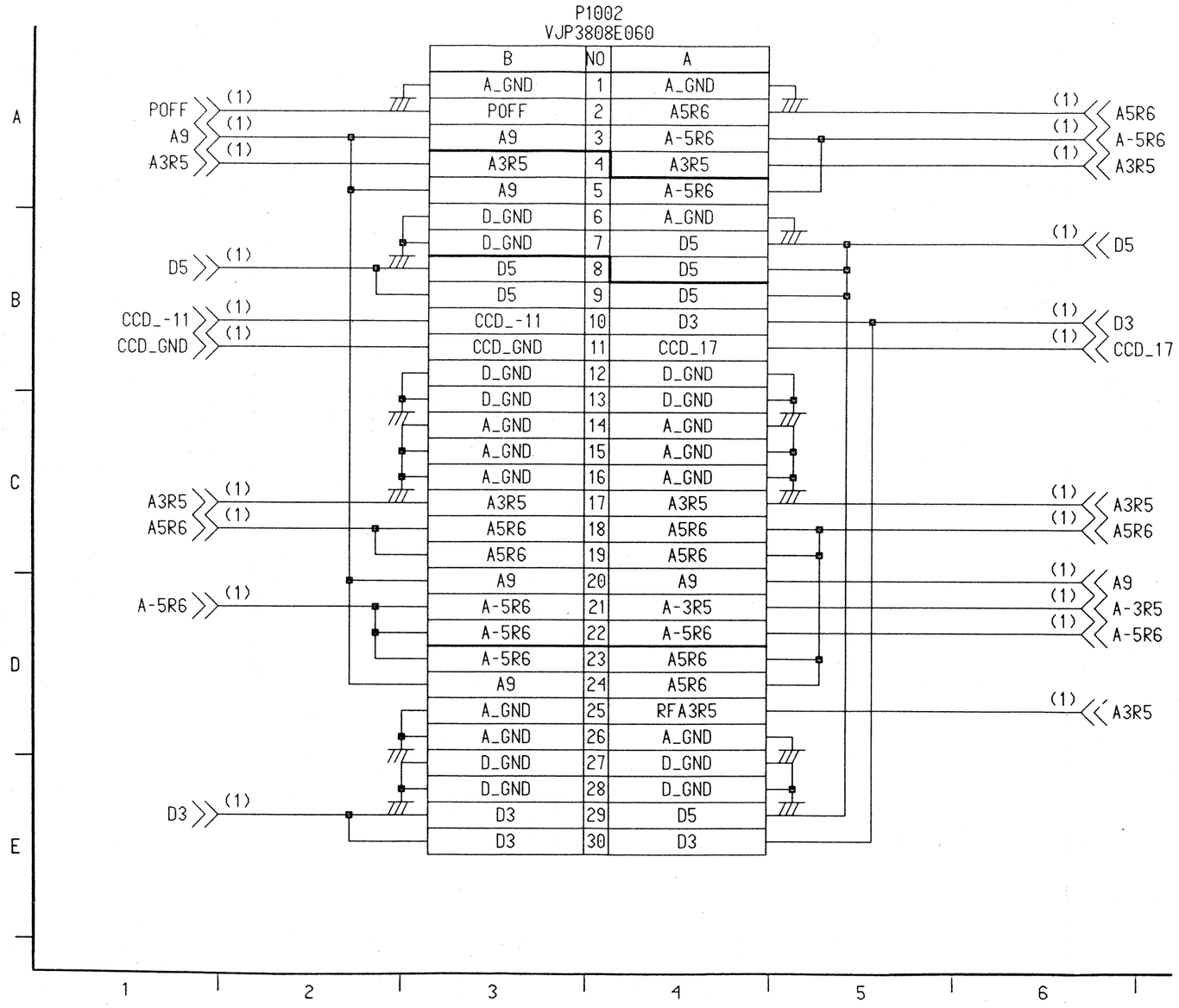
POWER (1/2) SCHEMATIC DIAGRAM



REVERSE SIDE

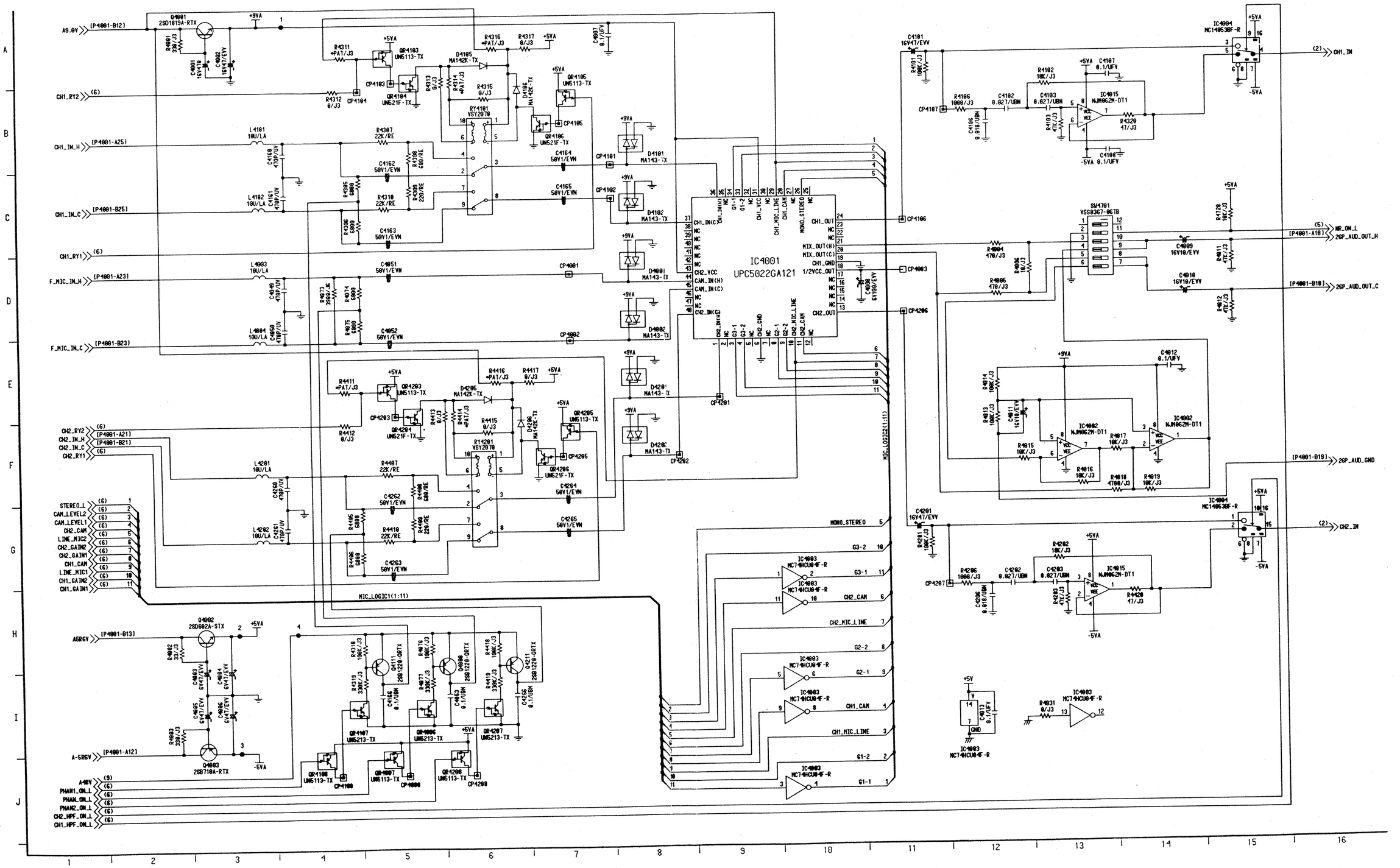
VIDEO MAIN 7/7

POWER (2/2) SCHEMATIC DIAGRAM



2—61

AUDIO LCD (1/9) AUDIO INPUT SCHEMATIC DIAGRAM

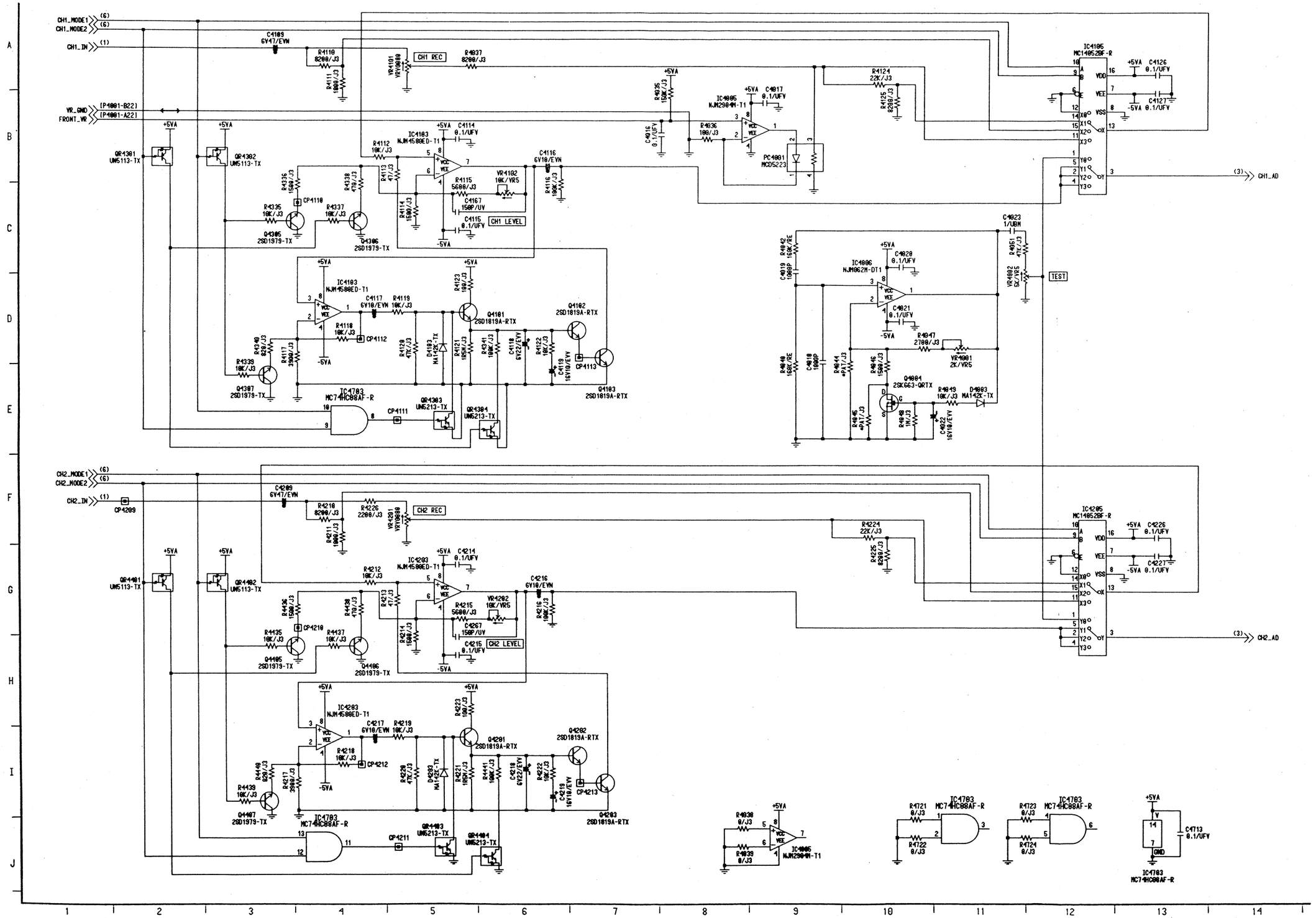


REVERSE SIDE

POWER 2/2

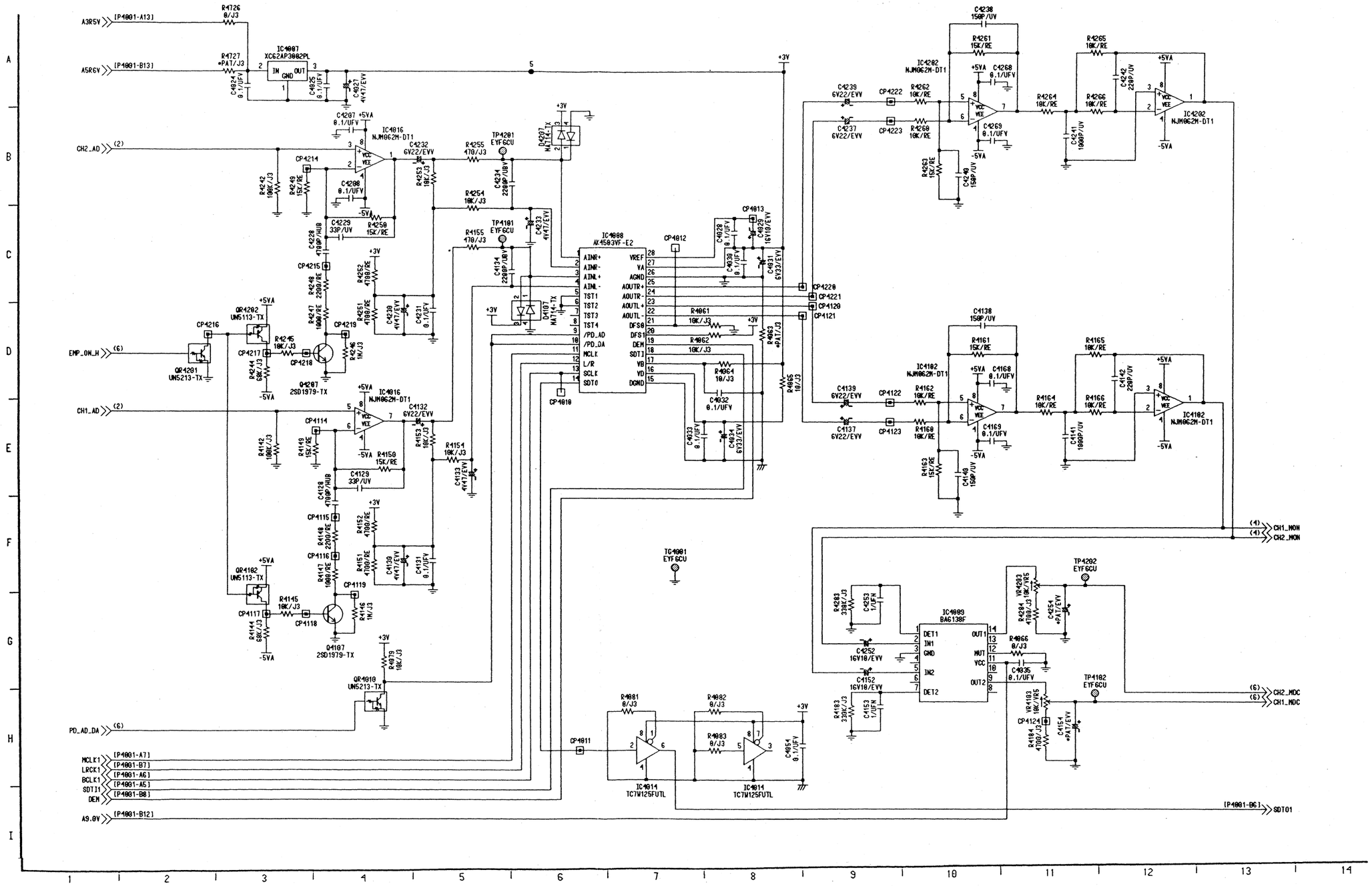
2—62

AUDIO LCD (2/9) AUDIO AGC SCHEMATIC DIAGRAM



2—63

AUDIO LCD (3/9) AUDIO A/D D/A SCHEMATIC DIAGRAM

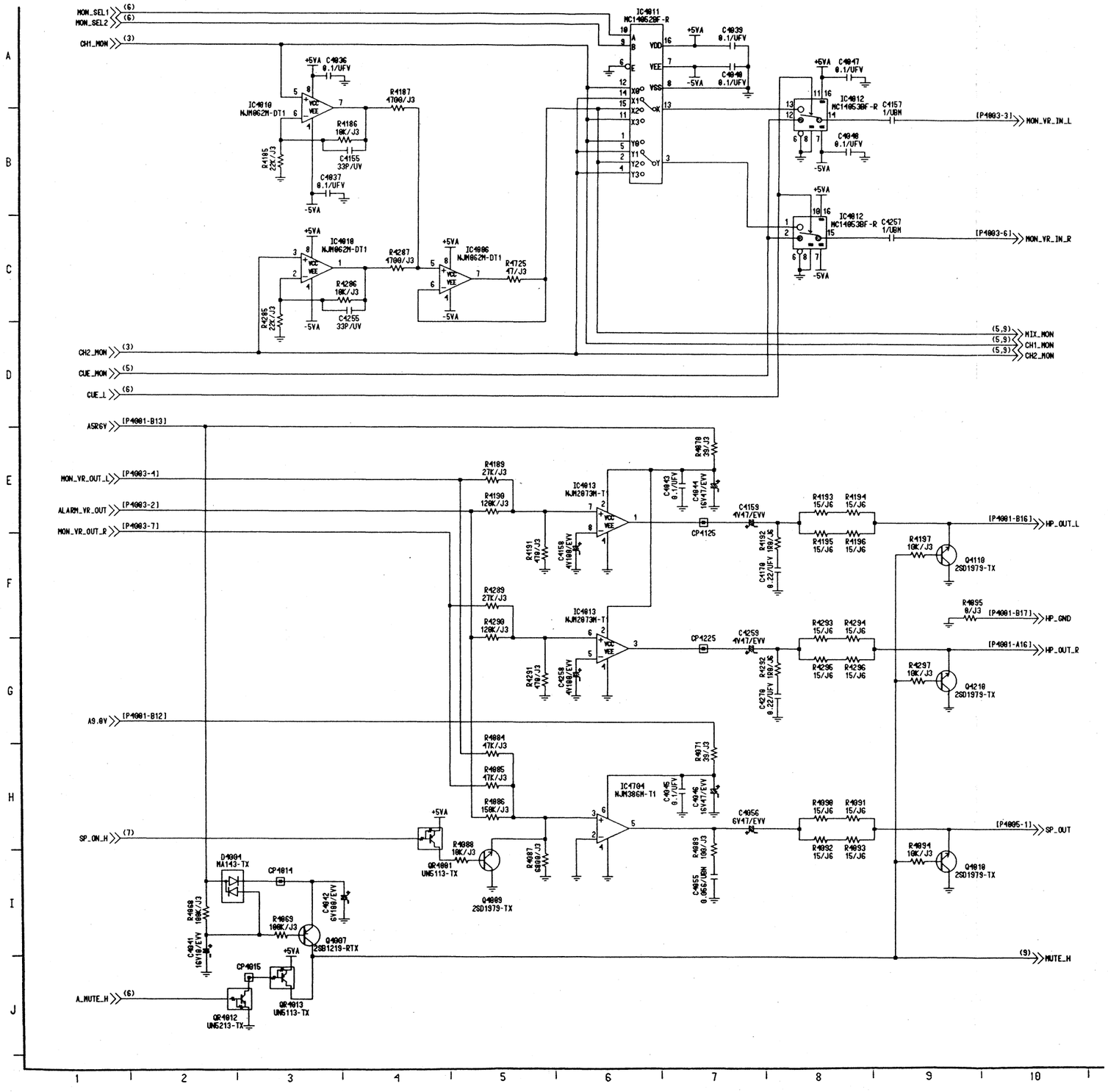


REVERSE SIDE

AUDIO LCD 2/9

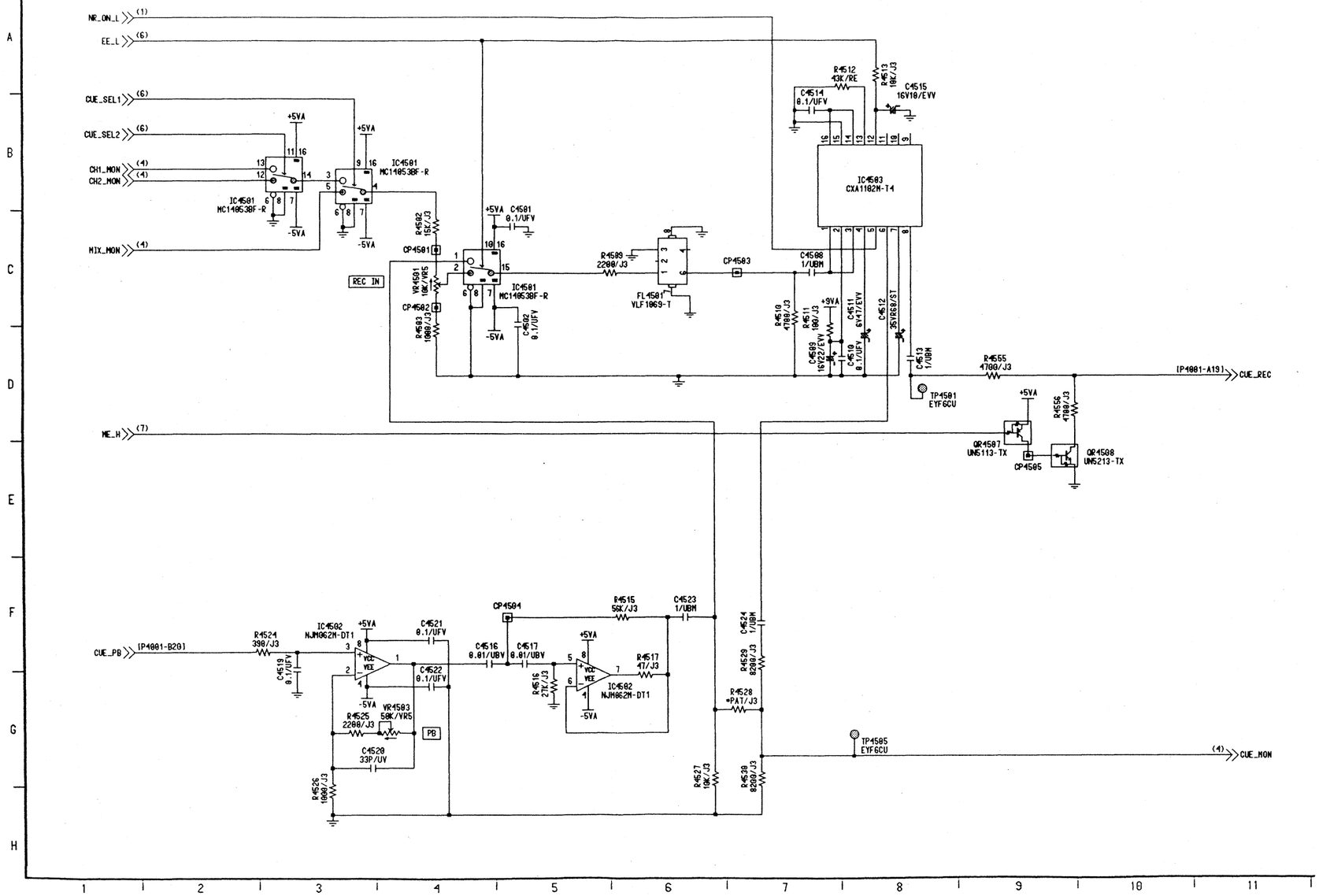
2—64

AUDIO LCD (4/9) AUDIO MONITOR SCHEMATIC DIAGRAM



2—65

AUDIO LCD (5/9) AUDIO CUE SCHEMATIC DIAGRAM

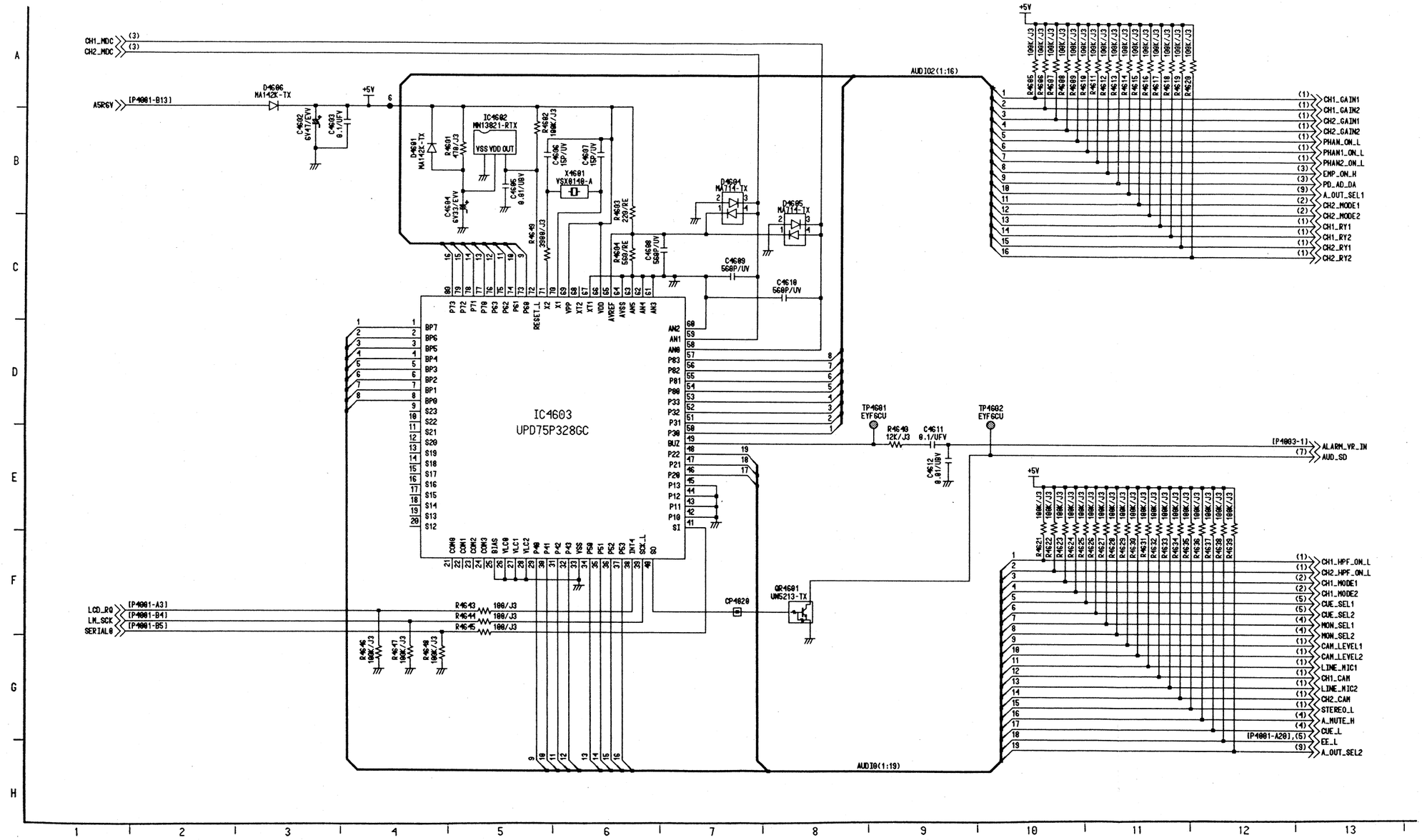


REVERSE SIDE

AUDIO LCD 4/9

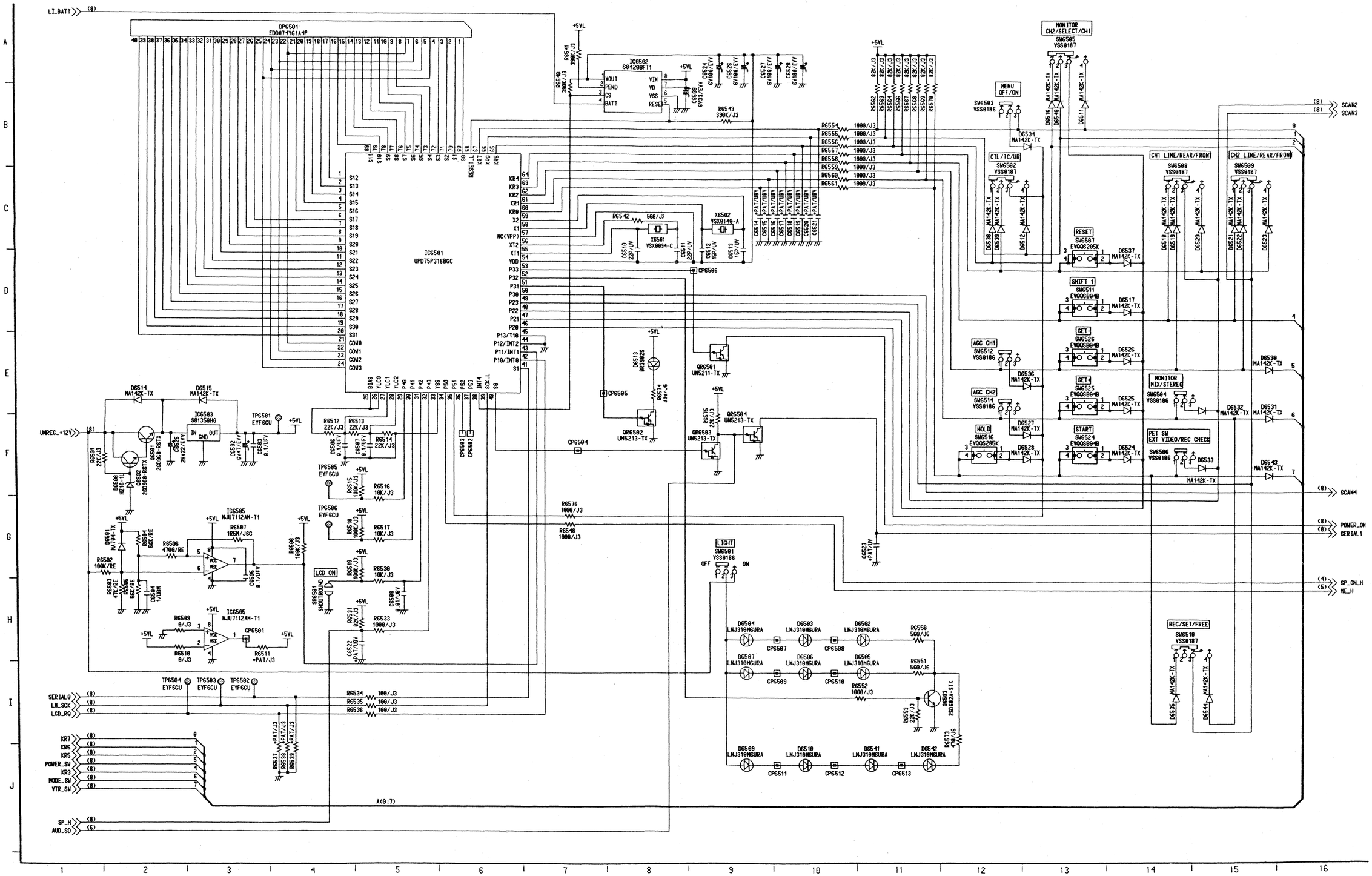
2—66

AUDIO LCD (6/9) AUDIO CONTROL SCHEMATIC DIAGRAM



2—67

AUDIO LCD (7/9) AUDIO LCD SCHEMATIC DIAGRAM

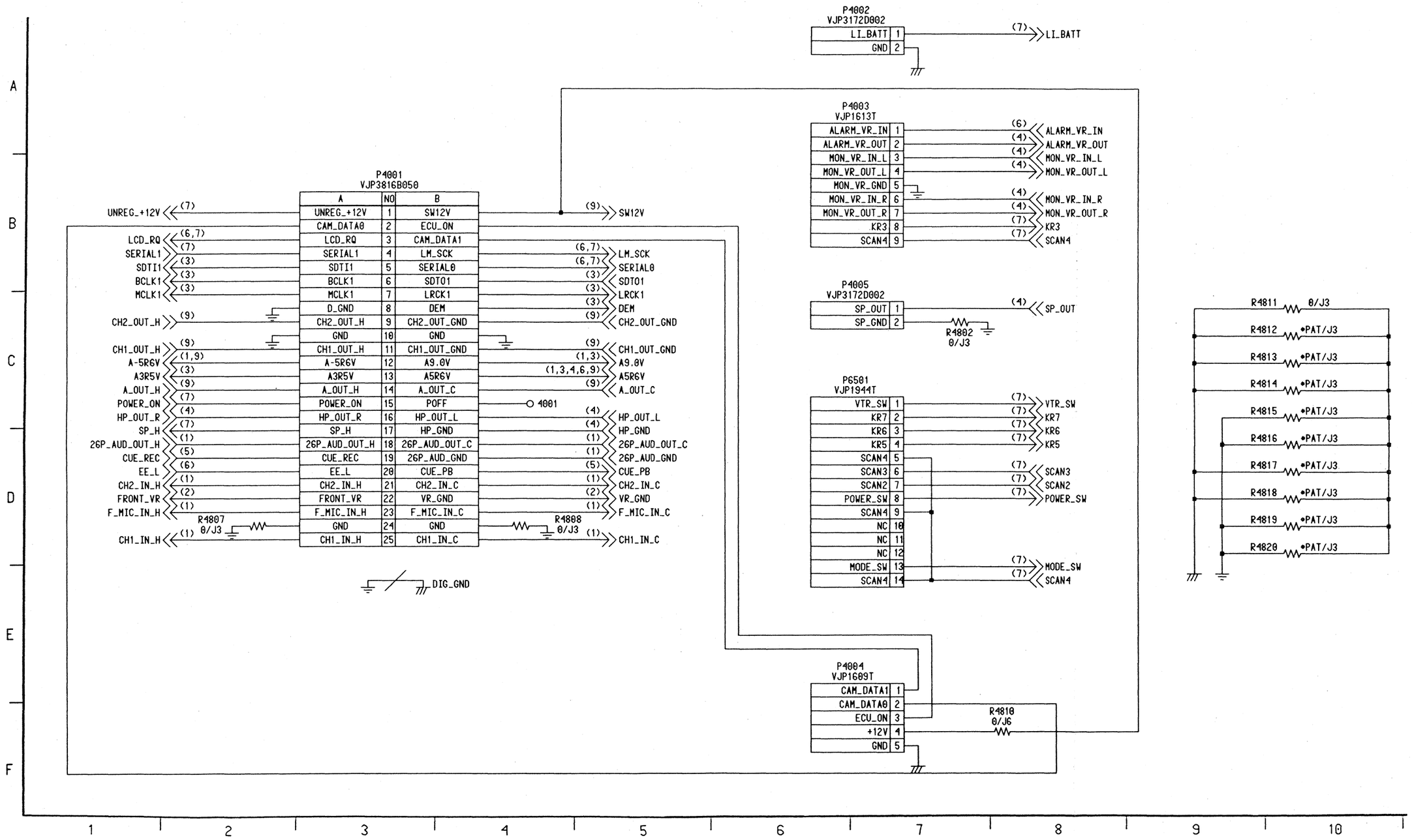


REVERSE SIDE

AUDIO LCD 6/9

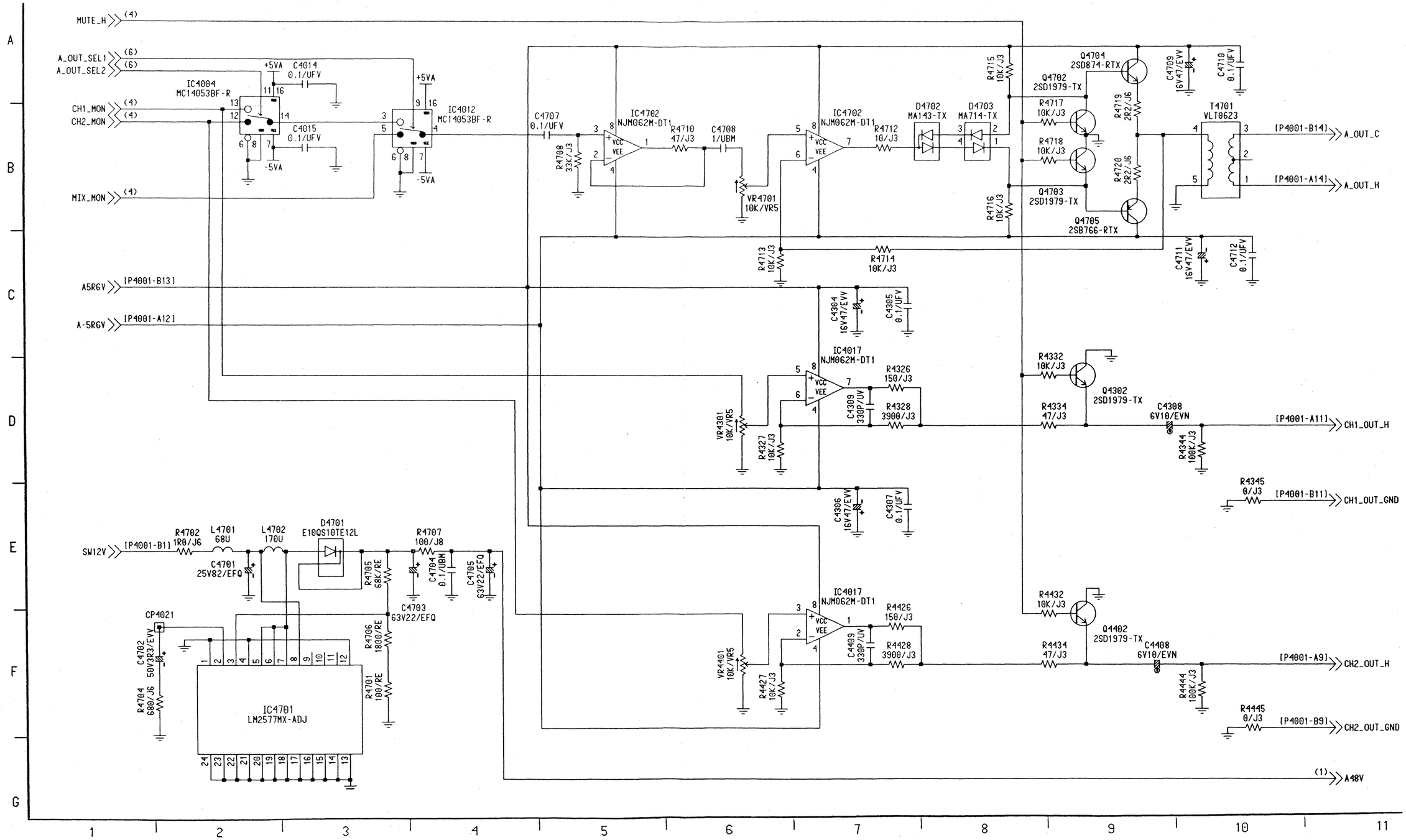
2—68

AUDIO LCD (8/9) AUDIO LCD I/F SCHEMATIC DIAGRAM



2—69

AUDIO LCD (9/9) AUDIO OUT SCHEMATIC DIAGRAM

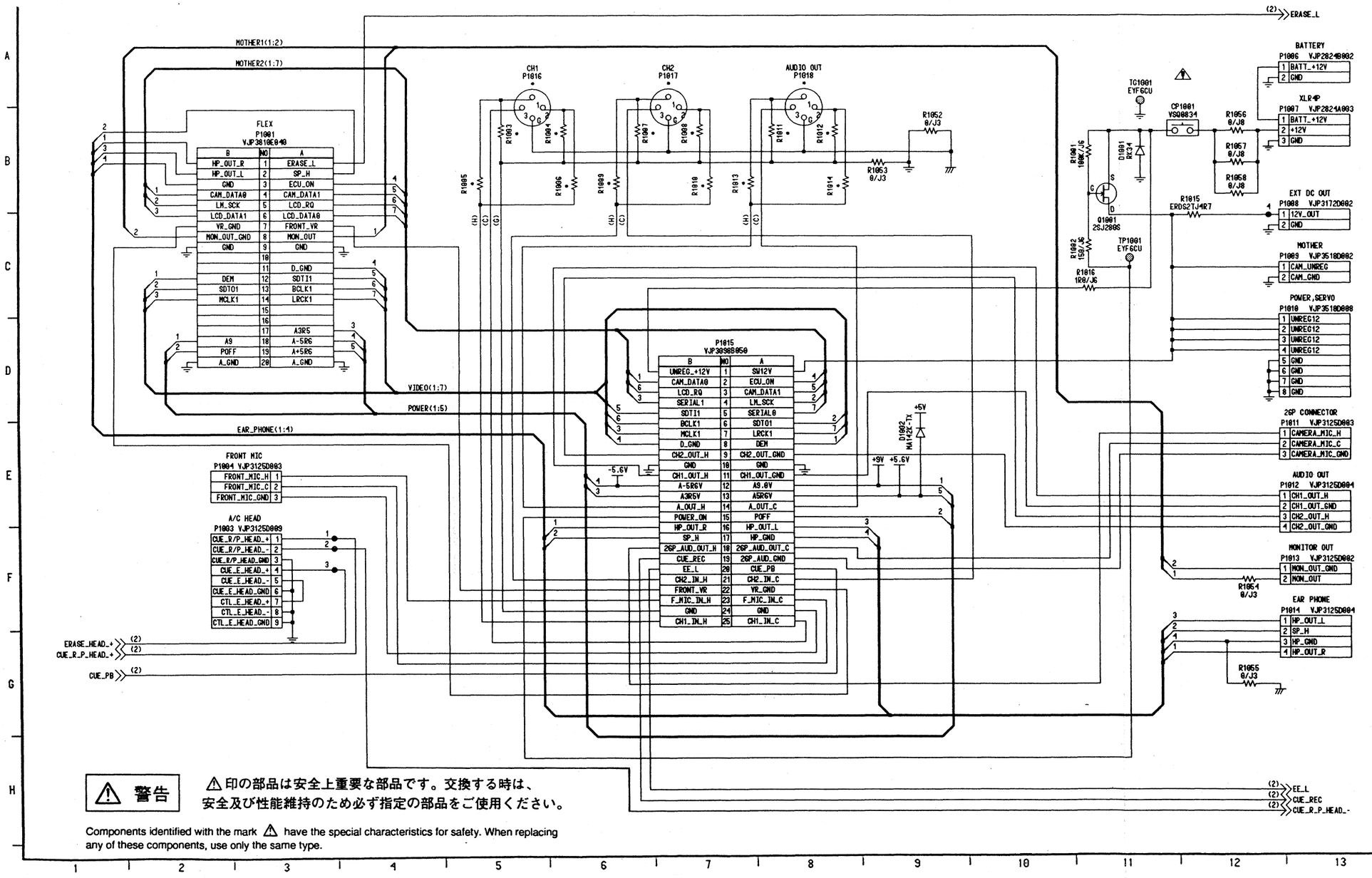


REVERSE SIDE

AUDIO LCD 8/9

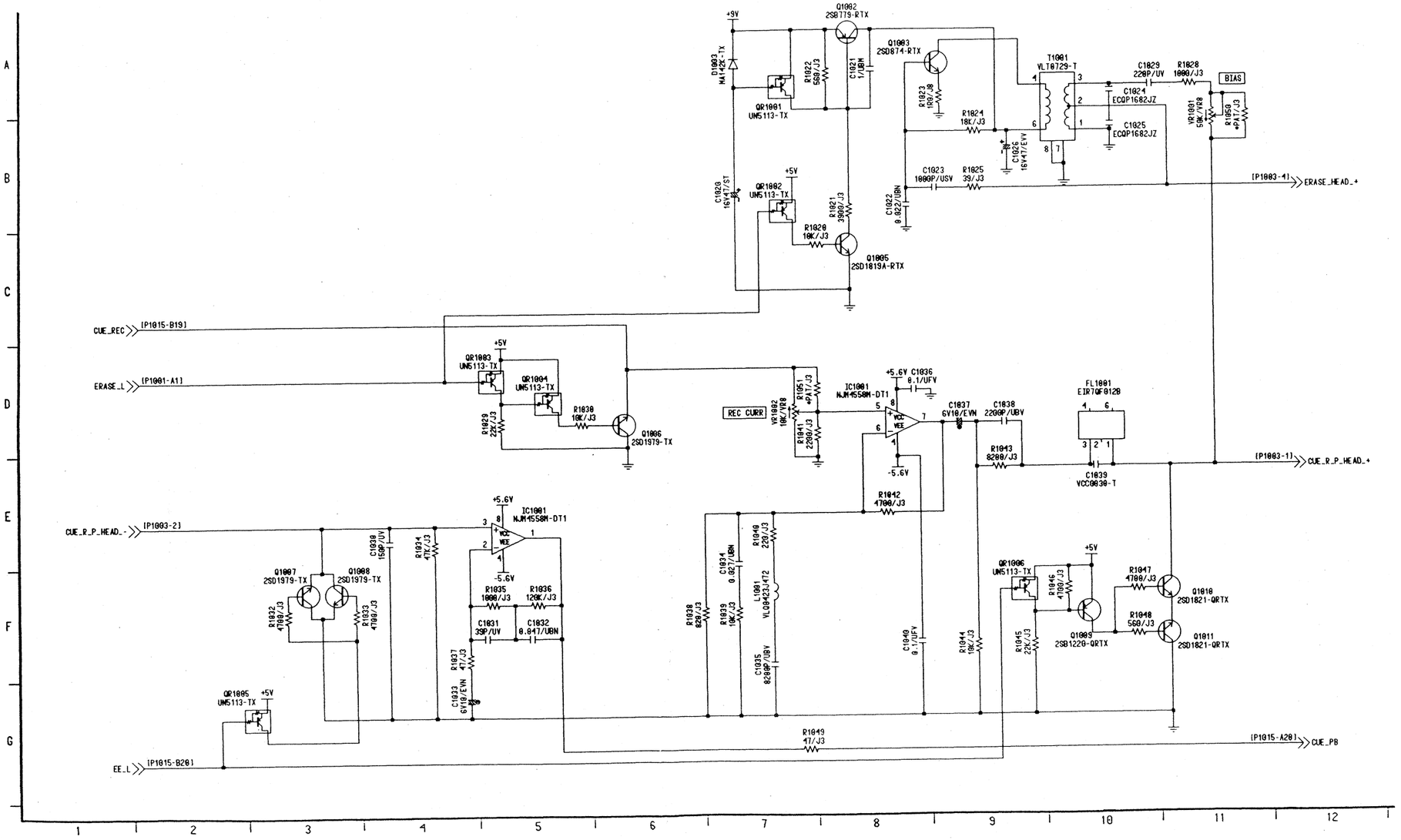
2—70

REAR JACK (1/3) SCHEMATIC DIAGRAM



2—71

REAR JACK (2/3) SCHEMATIC DIAGRAM



REVERSE SIDE

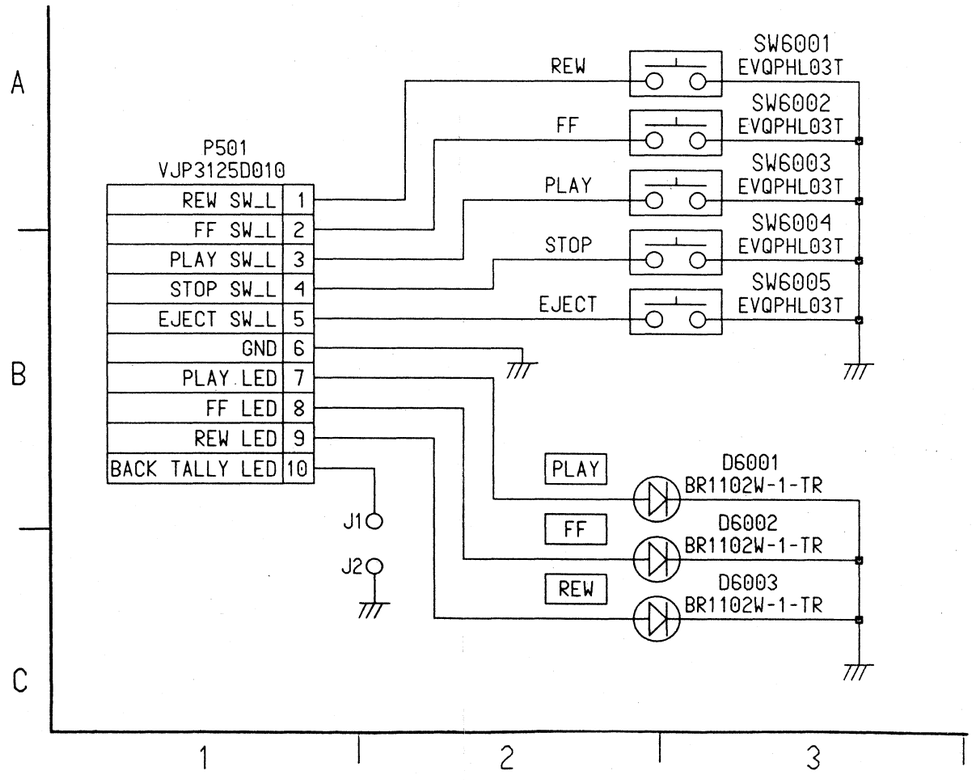
REAR JACK 1/3

2—72

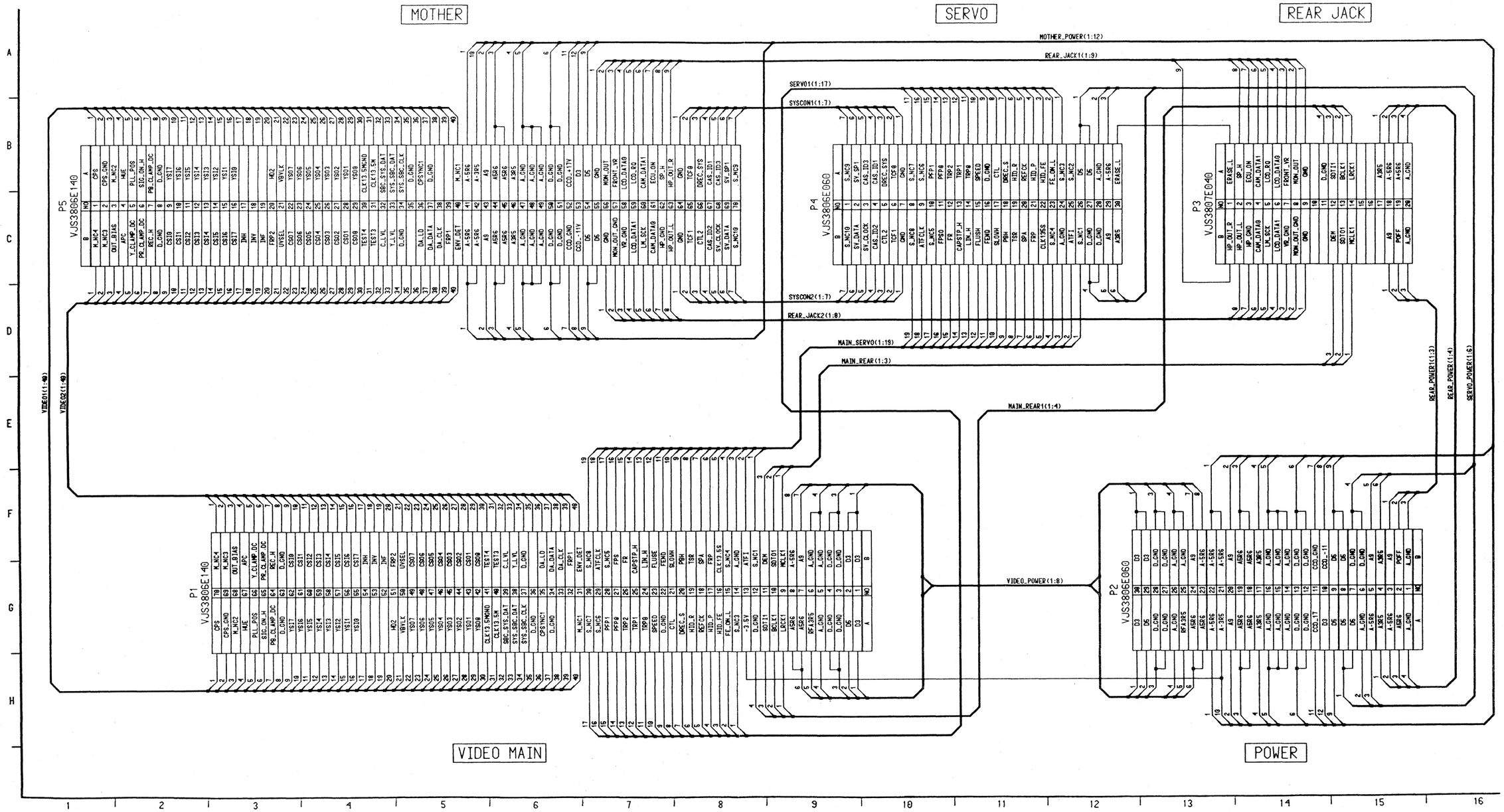
REAR JACK (3/3) COMPARISON CHART BETWEEN MODELS

REF	T	P. E	ON
P1016	VJP3551	VJS3551	VJP3551
P1017	VJP3551	VJS3551	VJP3551
P1018	VJS3551	VJP3551	VJS3551
R1003	*PAT/J3	0/J3	0/J3
R1004	0/J3	*PAT/J3	0/J3
R1005	0/J3	*PAT/J3	0/J3
R1006	*PAT/J3	0/J3	0/J3
R1007	*PAT/J3	0/J3	0/J3
R1008	0/J3	*PAT/J3	0/J3
R1009	0/J3	*PAT/J3	0/J3
R1010	*PAT/J3	0/J3	0/J3
R1011	0/J3	*PAT/J3	0/J3
R1012	*PAT/J3	0/J3	0/J3
R1013	*PAT/J3	0/J3	0/J3
R1014	0/J3	*PAT/J3	0/J3
R1041	*PAT/J3	*PAT/J3	0/J3
R1050	*PAT/J3	*PAT/J3	0/J3
R1051	*PAT/J3	*PAT/J3	0/J3

OPERATION SCHEMATIC DIAGRAM



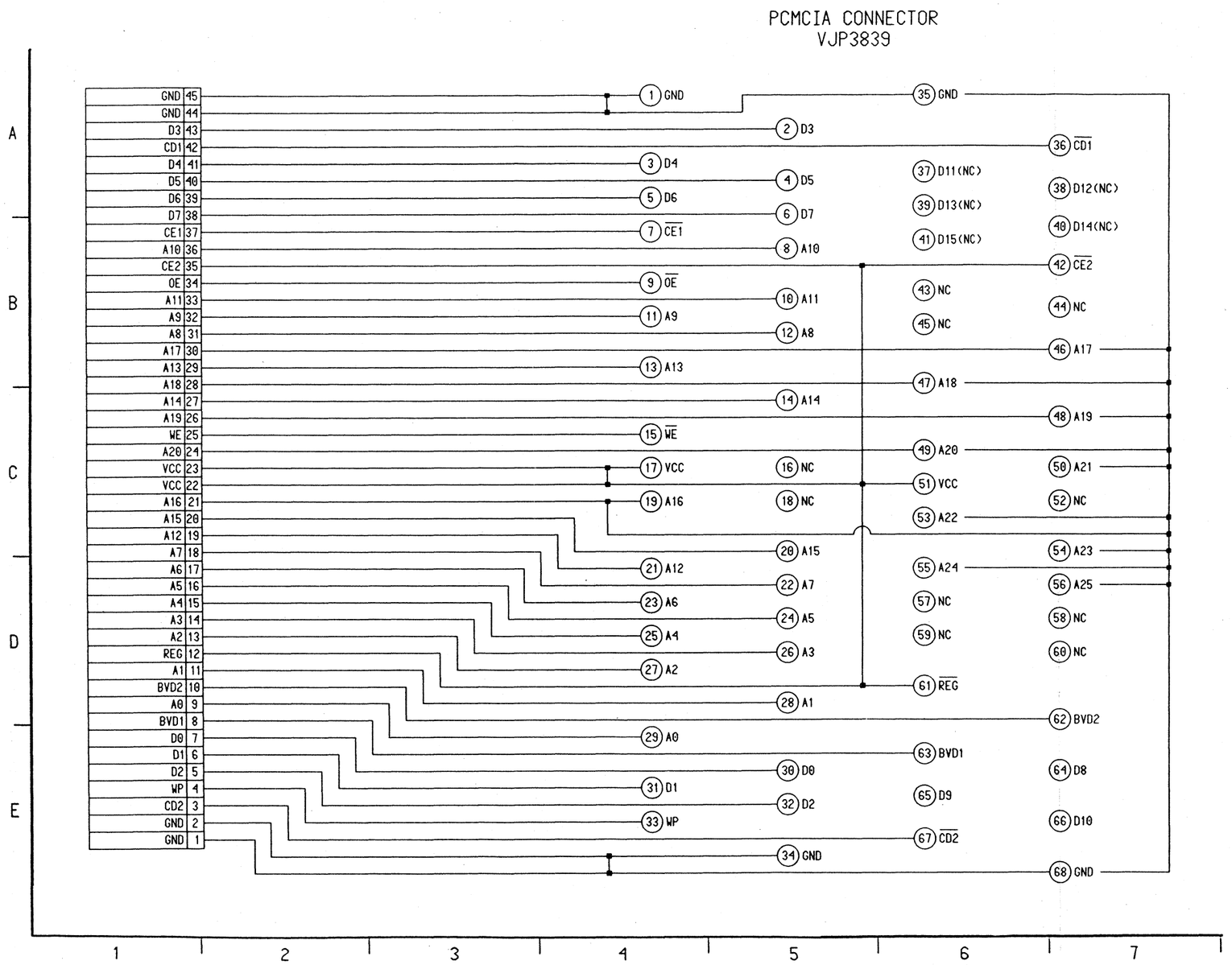
VTR FLEX SCHEMATIC DIAGRAM



REVERSE SIDE

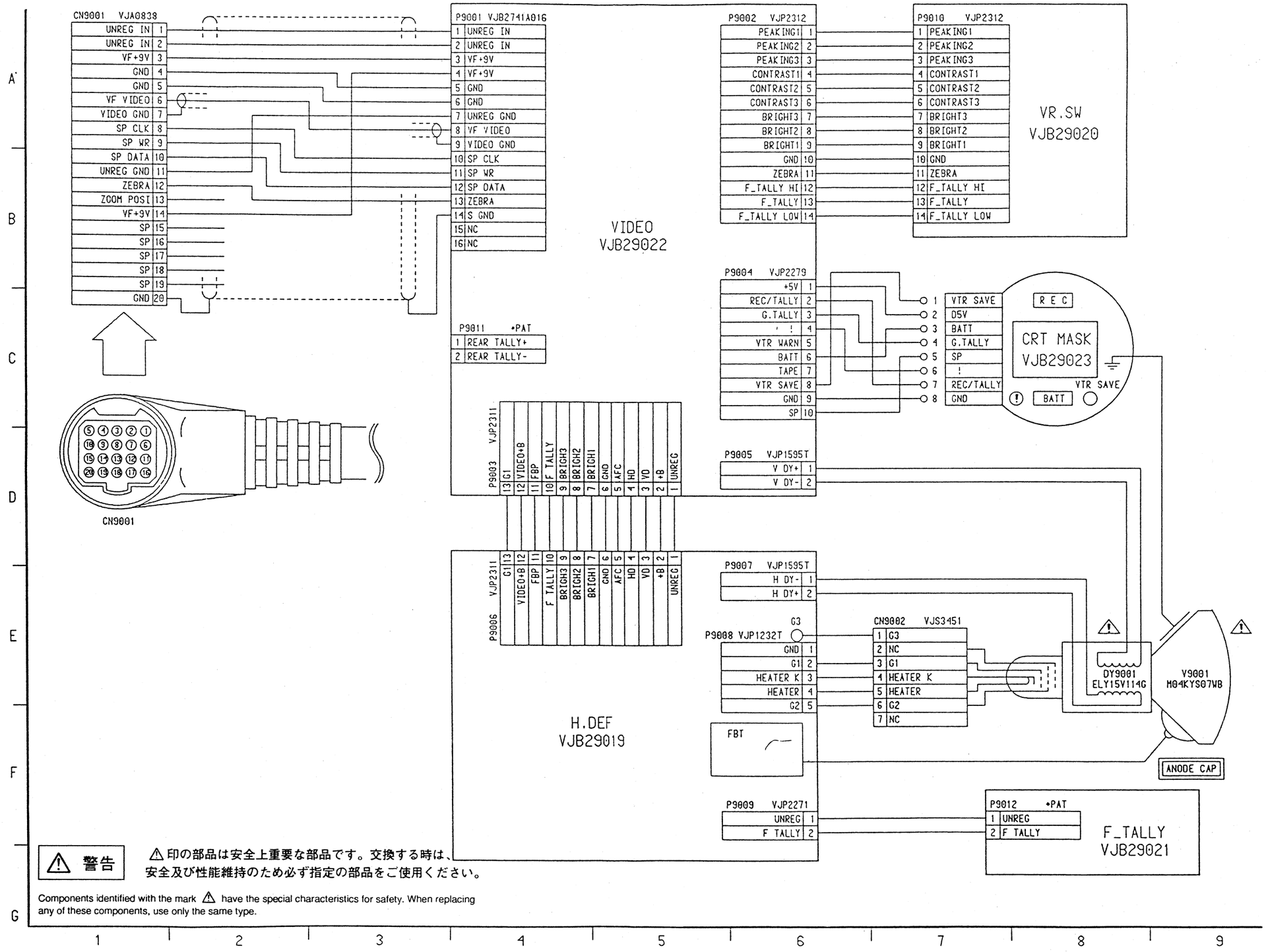
REAR JACK 3/3, OPERATE

MEMORY CARD FLEX SCHEMATIC DIAGRAM



2—75

EVF INTERCONNECTION



⚠ 警告

⚠印の部品は安全上重要な部品です。交換する時は、安全及び性能維持のため必ず指定の部品をご使用ください。

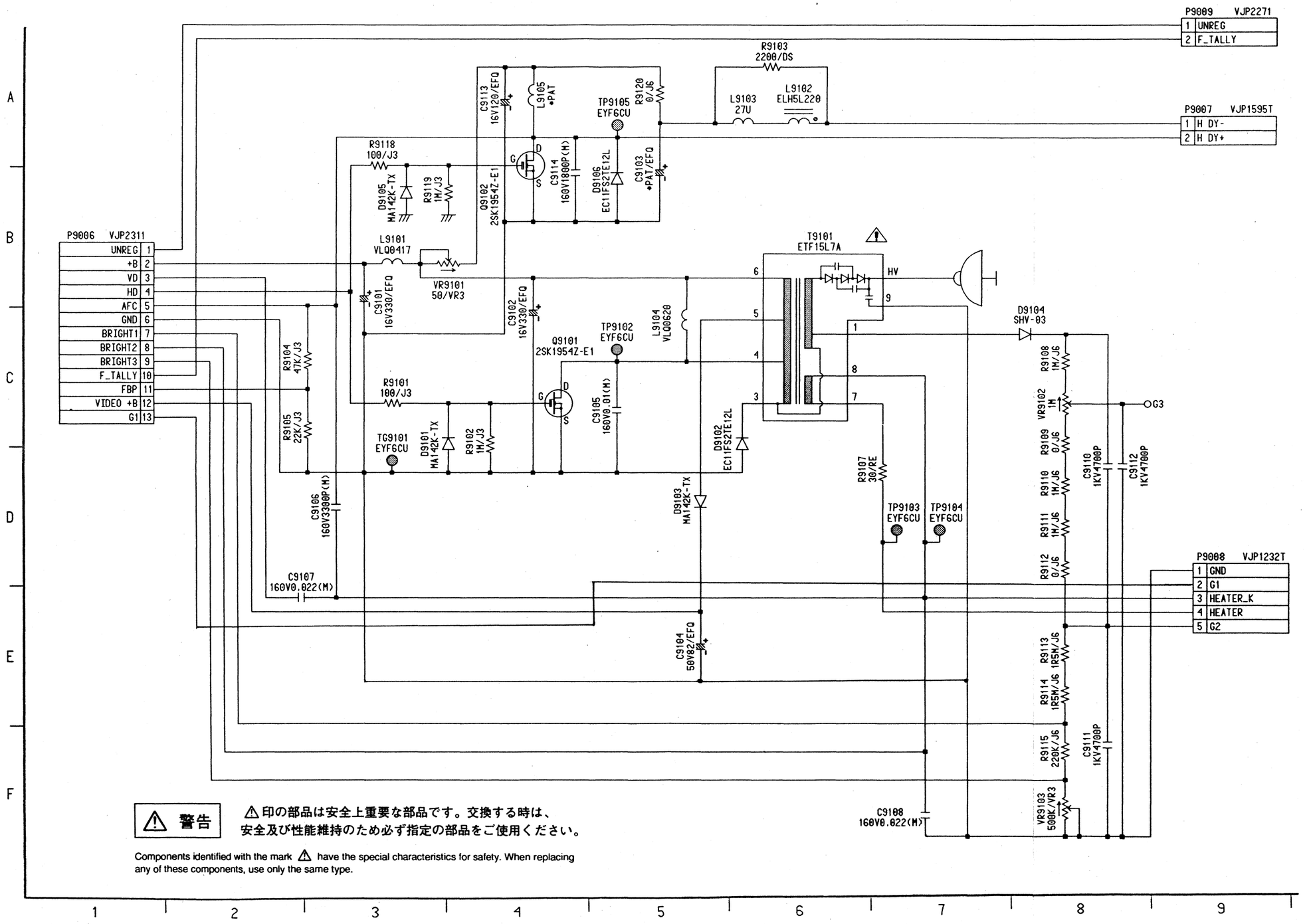
Components identified with the mark ⚠ have the special characteristics for safety. When replacing any of these components, use only the same type.

REVERSE SIDE

MEMORY CARD FLEX

2—76

H. DEF SCHEMATIC DIAGRAM



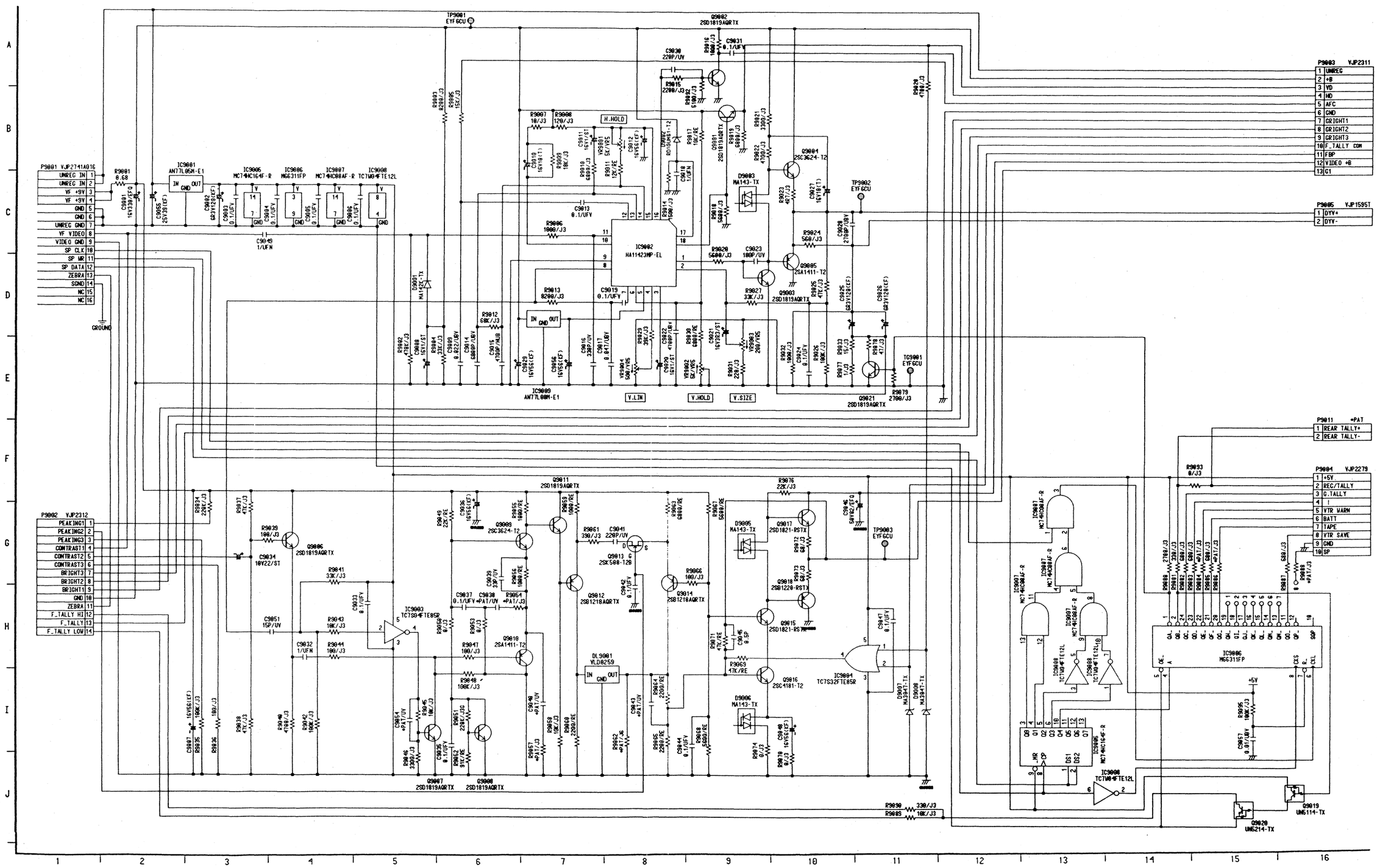
⚠ 警告

⚠印の部品は安全上重要な部品です。交換する時は、
安全及び性能維持のため必ず指定の部品をご使用ください。

Components identified with the mark ⚠ have the special characteristics for safety. When replacing any of these components, use only the same type.

2—77

EVF VIDEO SCHEMATIC DIAGRAM

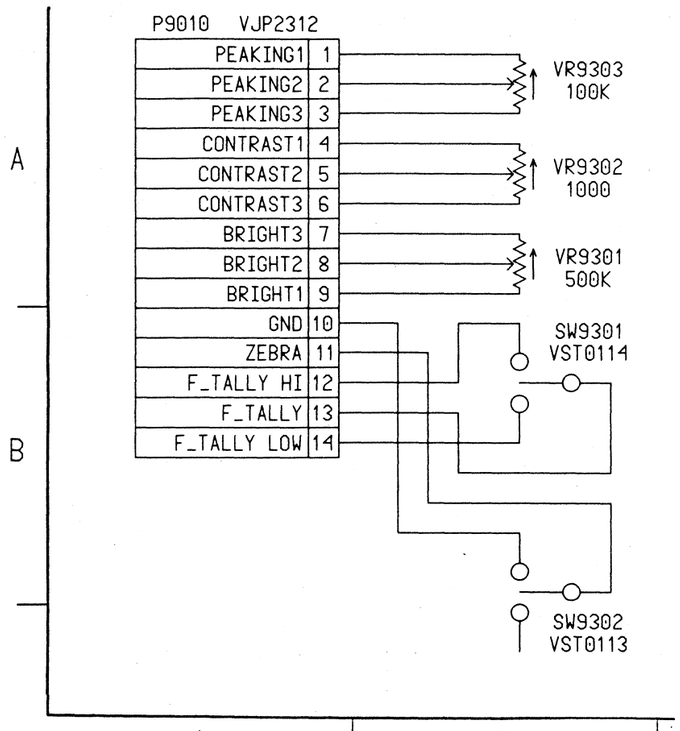


REVERSE SIDE

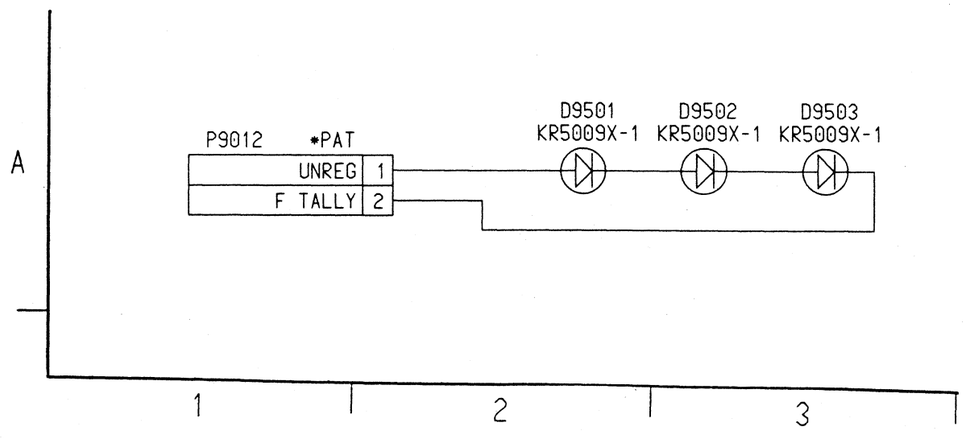
H DEF

2—78

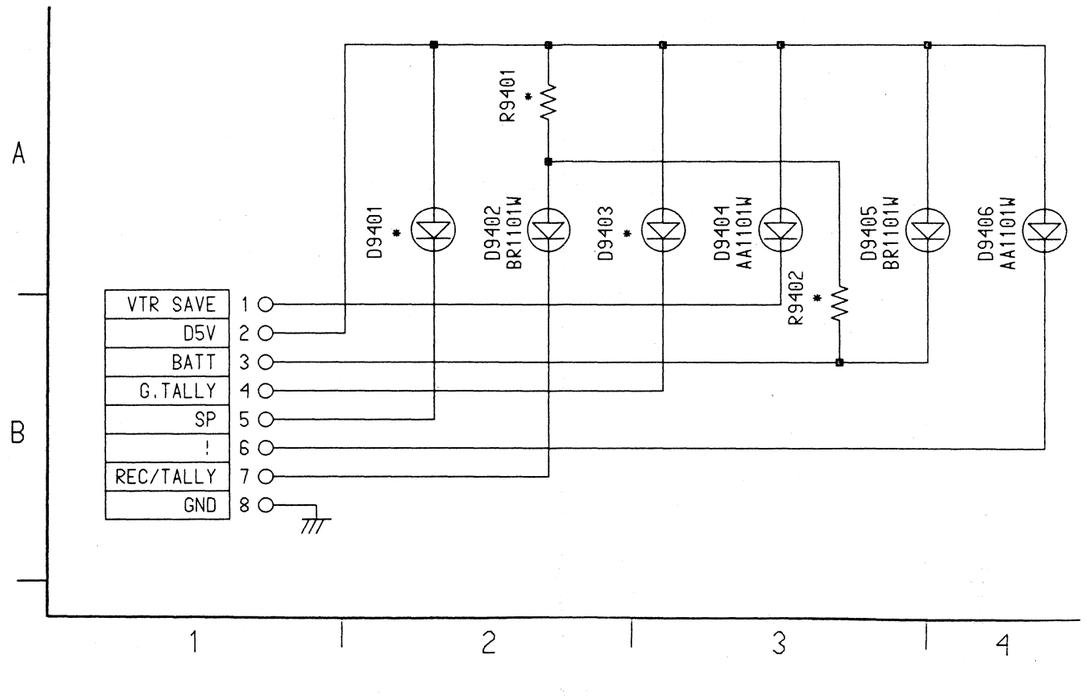
EVF SWVR SCHEMATIC DIAGRAM



F TALLY SCHEMATIC DIAGRAM



EVF CRT MASK SCHEMATIC DIAGRAM

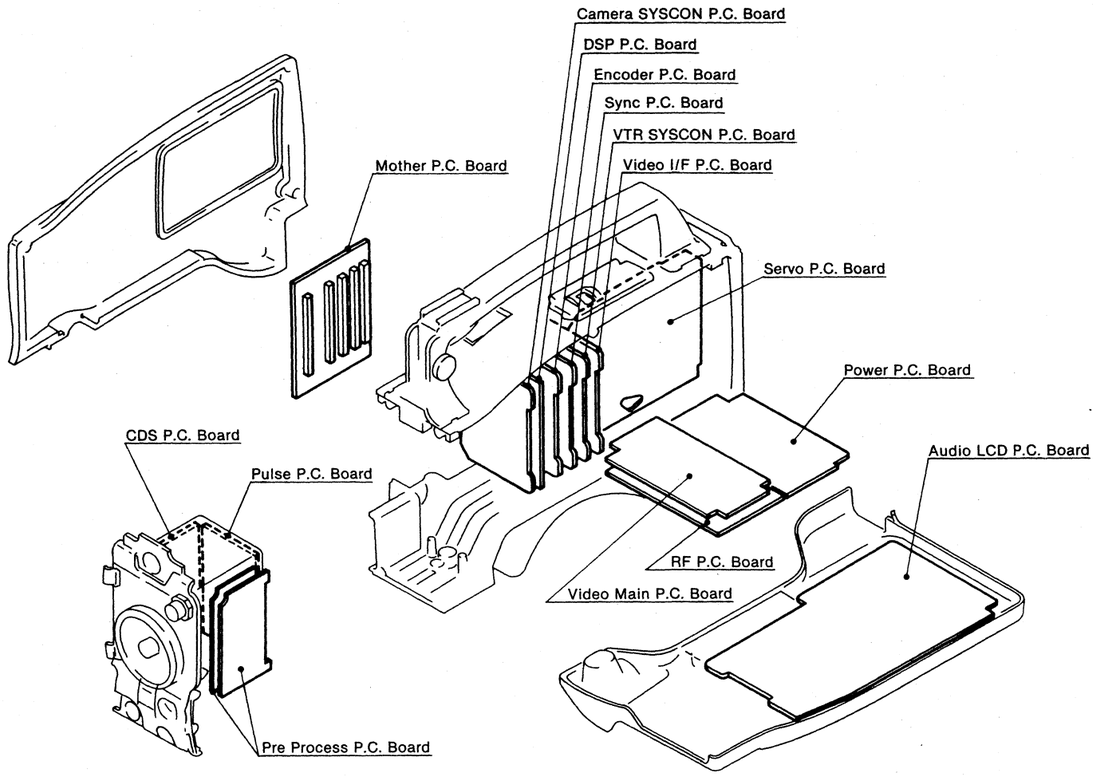


SECTION 3

CIRCUIT BOARDS

CONTENTS

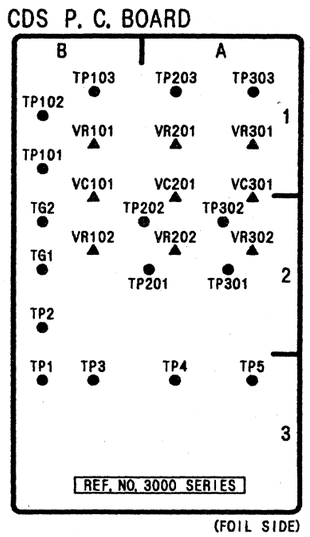
P.C. BOARD LOCATION

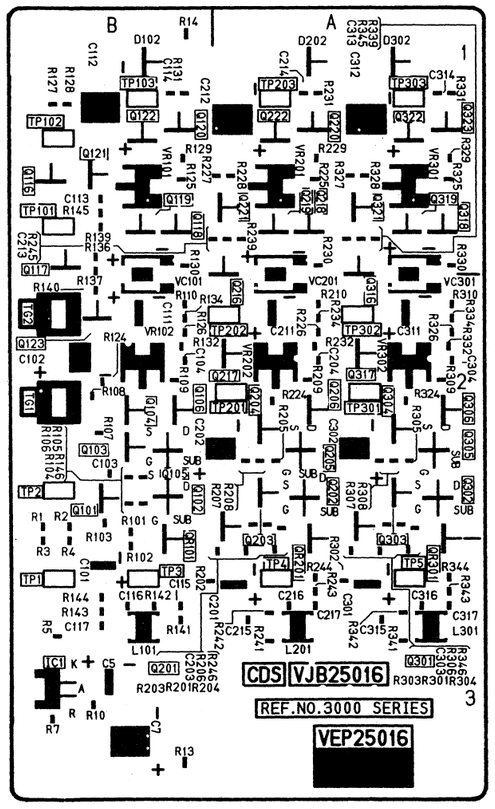


CDS								
Transistors		Q3204	A-2 (F)	Q3311	A-2 (C)	TP3004	A-3 (F)
Q3001	B-3 (C)	Q3205	A-2 (F)	Q3312	A-2 (C)	TP3005	A-3 (F)
Q3101	B-2 (F)	Q3206	A-2 (F)	Q3313	A-2 (C)	TP3101	B-1 (F)
Q3102	B-2 (F)	Q3207	A-3 (C)	Q3314	A-2 (C)	TP3102	B-1 (F)
Q3103	B-2 (F)	Q3208	A-2 (C)	Q3315	A-1 (C)	TP3103	B-1 (F)
Q3104	B-2 (F)	Q3209	A-2 (C)	Q3316	A-2 (F)	TP3201	A-2 (F)
Q3105	B-2 (F)	Q3210	A-2 (C)	Q3317	A-2 (F)	TP3202	A-2 (F)
Q3106	B-2 (F)	Q3211	A-2 (C)	Q3318	A-1 (F)	TP3203	A-1 (F)
Q3107	B-3 (C)	Q3212	A-2 (C)	Q3319	A-1 (F)	TP3301	A-2 (F)
Q3108	B-2 (C)	Q3213	A-2 (C)	Q3321	A-1 (F)	TP3302	A-2 (F)
Q3109	B-2 (C)	Q3214	A-2 (C)	Q3322	A-1 (F)	TP3303	A-1 (F)
Q3110	B-2 (C)	Q3215	A-1 (C)	Q3323	A-1 (F)	TG3001	B-2 (F)
Q3111	B-2 (C)	Q3216	A-2 (F)	**Transistor-Resistors**		TG3002	B-2 (F)
Q3112	B-2 (C)	Q3217	A-2 (F)			**Adjustments**	
Q3113	B-1 (C)	Q3218	A-1 (F)	QR3101	B-3 (F)		
Q3114	B-2 (C)	Q3219	A-1 (F)	QR3102	B-3 (C)	VC3101	B-2 (F)
Q3115	B-1 (C)	Q3220	A-1 (F)	QR3201	A-3 (F)	VC3201	A-2 (F)
Q3116	B-1 (F)	Q3221	A-1 (F)	QR3202	A-3 (C)	VC3301	A-2 (F)
Q3117	B-1 (F)	Q3222	A-1 (F)	QR3301	A-3 (F)	VR3101	B-1 (F)
Q3118	B-1 (F)	Q3301	A-3 (F)	QR3302	A-3 (C)	VR3102	B-2 (F)
Q3119	B-1 (F)	Q3302	A-2 (F)	**Integrated Circuit**		VR3201	B-1 (F)
Q3120	B-1 (F)	Q3303	A-2 (F)			VR3202	A-2 (F)
Q3121	B-1 (F)	Q3304	A-2 (F)	IC3001	B-3 (F)	VR3301	A-1 (F)
Q3122	B-1 (F)	Q3305	A-2 (F)	IC3002	B-3 (C)	VR3302	A-2 (F)
Q3123	B-2 (F)	Q3306	A-2 (F)	**Test Points**		**Connectors**	
Q3201	B-3 (F)	Q3307	A-3 (C)				
Q3202	A-2 (F)	Q3308	A-2 (C)	TP3001	B-3 (F)	P3001	A-3 (C)
Q3203	A-2 (F)	Q3309	A-2 (C)	TP3002	B-2 (F)	P3002	B-2 (C)
		Q3310	A-2 (C)	TP3003	B-3 (F)	P3003	A-1 (C)

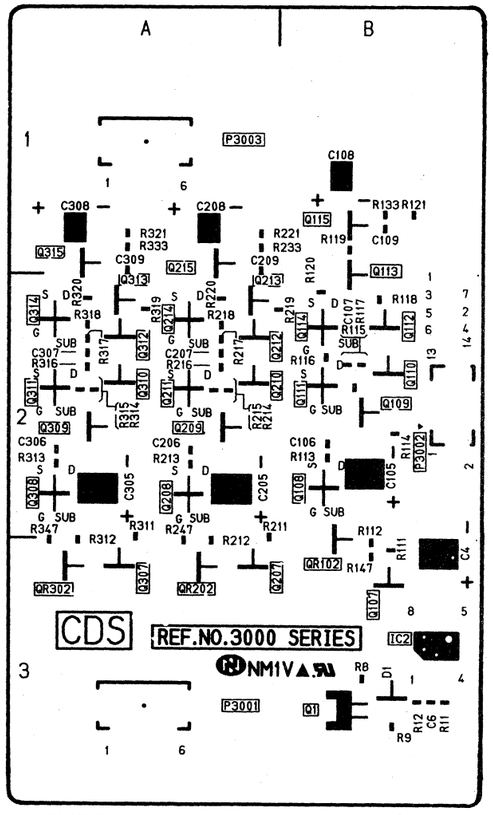
ADDRESS INFORMATION
(C)... COMPONENT SIDE
(F)... FOIL SIDE

CDS P.C. BOARD (VEP25016A)





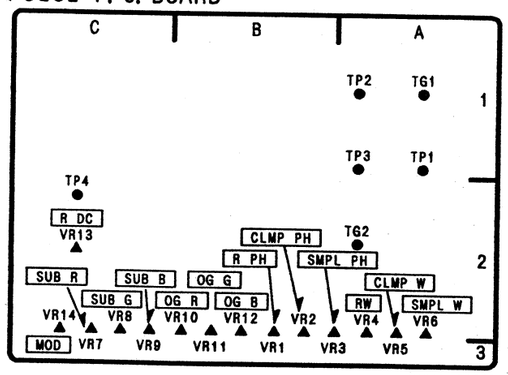
(FIOL SIDE)



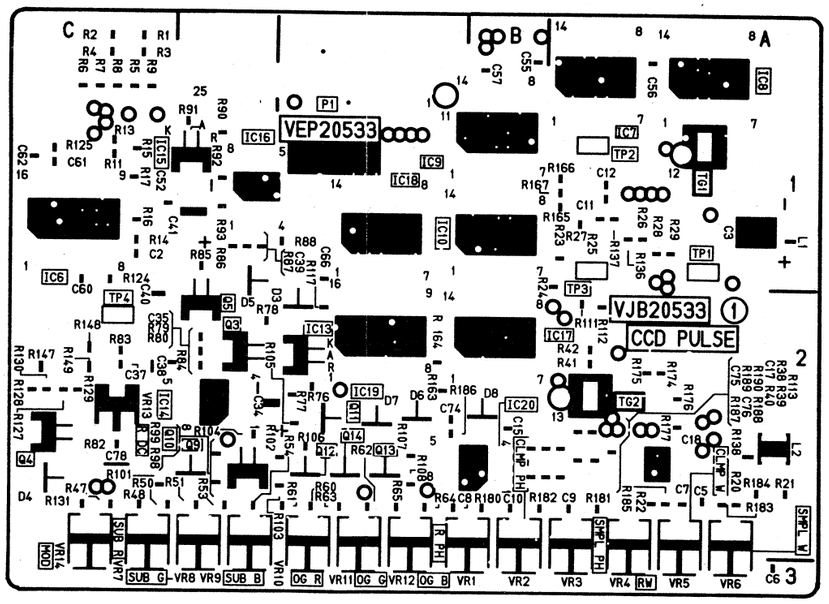
(COMPONENT SIDE)

PULSE P.C. BOARD (VEP20533A)

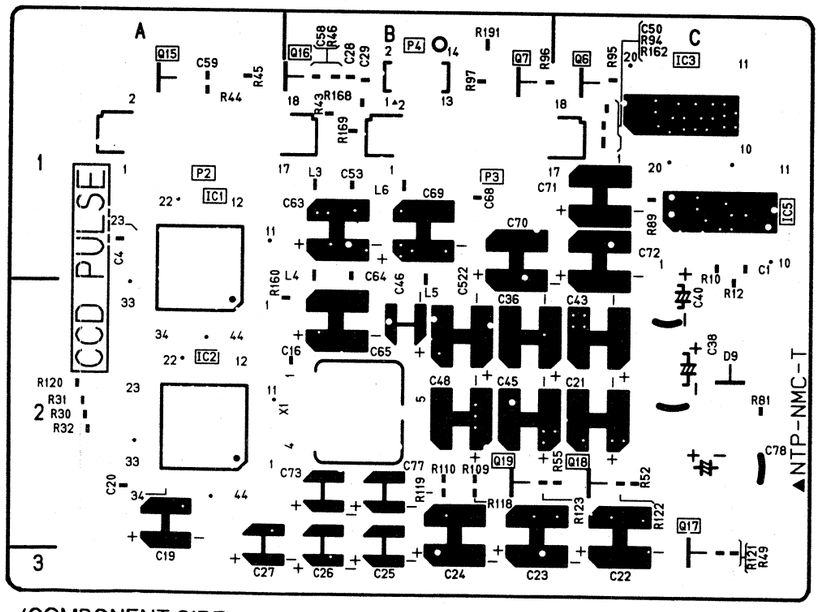
PULSE P. C. BOARD



(FOIL SIDE)



(FIOL SIDE)



(COMPONENT SIDE)

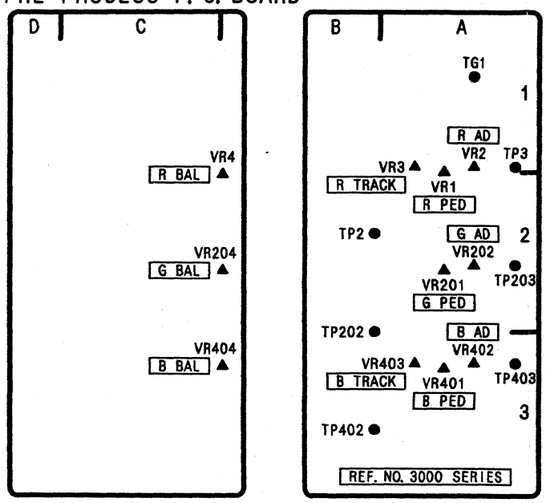
PULSE		
Transistors		
Q3	C-2	Ⓕ
Q4	C-2	Ⓕ
Q5	C-2	Ⓕ
Q6	C-1	Ⓒ
Q7	B-1	Ⓒ
Q9	C-2	Ⓕ
Q10	C-2	Ⓕ
Q11	B-2	Ⓕ
Q12	B-2	Ⓕ
Q13	B-2	Ⓕ
Q14	B-2	Ⓕ
Q15	A-1	Ⓒ
Q16	B-1	Ⓒ
Q17	C-2	Ⓒ
Q18	C-2	Ⓒ
Q19	B-2	Ⓒ
Integrated Circuit		
IC1	A-1	Ⓒ
IC2	A-2	Ⓒ
IC3	C-1	Ⓒ
IC5	C-1	Ⓒ
IC6	C-1	Ⓕ
IC7	A-1	Ⓕ
IC8	A-1	Ⓕ
IC9	B-1	Ⓕ
IC10	B-1	Ⓕ
IC13	B-2	Ⓕ
IC14	C-2	Ⓕ
IC15	C-1	Ⓕ
IC16	C-1	Ⓕ
IC17	A-2	Ⓕ
IC18	B-1	Ⓕ
IC19	B-2	Ⓕ
IC20	B-2	Ⓕ
Test Points		
TP1	A-1	Ⓕ
TP2	A-1	Ⓕ
TP3	A-1	Ⓕ
TP4	C-2	Ⓕ
TG1	A-2	Ⓕ
TG2	A-2	Ⓕ
Adjustment		
VR1	B-3	Ⓕ
VR2	B-3	Ⓕ
VR3	A-3	Ⓕ
VR4	A-3	Ⓕ
VR5	A-3	Ⓕ
VR6	A-3	Ⓕ
VR7	C-3	Ⓕ
VR8	C-3	Ⓕ
VR9	C-3	Ⓕ
VR10	B-3	Ⓕ
VR11	B-3	Ⓕ
VR12	B-3	Ⓕ
VR13	C-2	Ⓕ
VR14	C-3	Ⓕ
Connectors		
P1	B-1	Ⓕ
P2	A-1	Ⓒ
P3	B-1	Ⓒ
P4	B-1	Ⓒ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

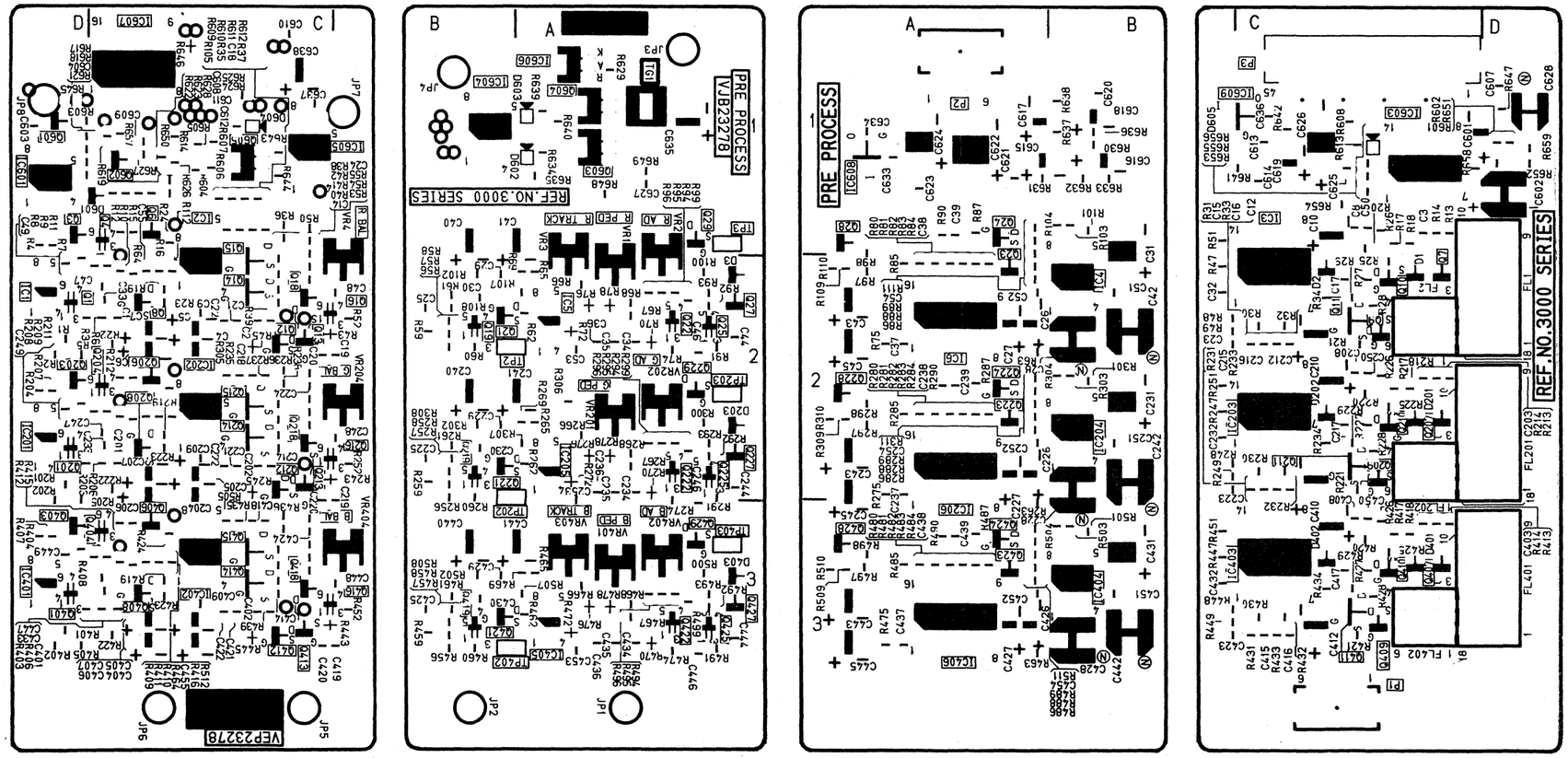
3—2

PRE PROCESS P.C. BOARD (VEP23278A)

PRE PROCESS P. C. BOARD



(FOIL SIDE)



(FOIL SIDE) (COMPONENT SIDE)

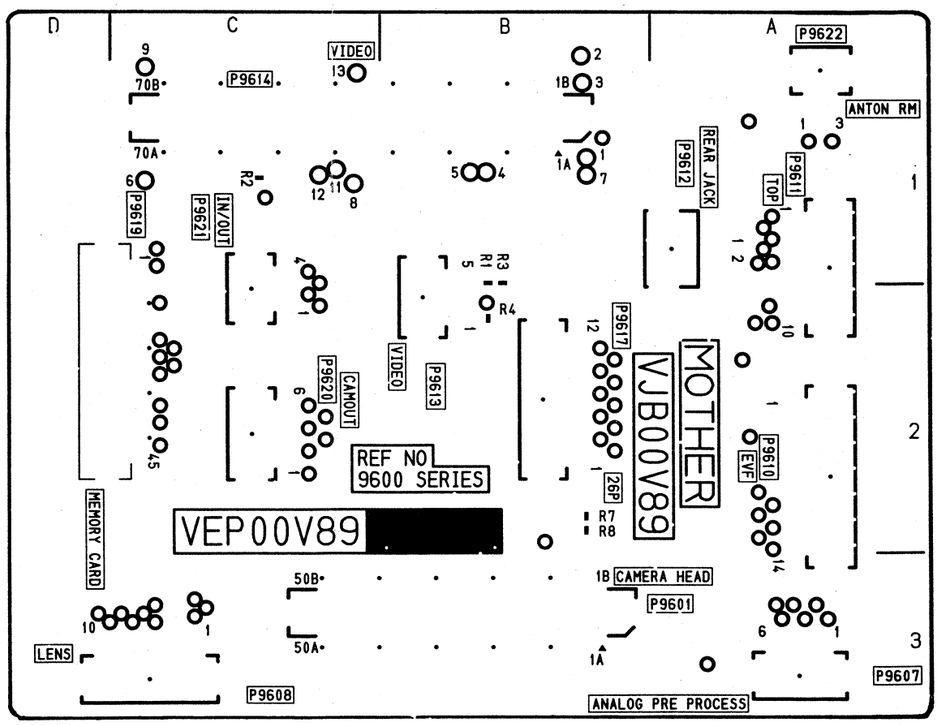
PRE PROCESS		
Transistors		
Q3001	D-1	Ⓕ
Q3003	C-1	Ⓕ
Q3004	C-1	Ⓕ
Q3006	C-2	Ⓒ
Q3007	C-2	Ⓕ
Q3008	C-2	Ⓒ
Q3009	C-2	Ⓒ
Q3010	C-2	Ⓒ
Q3011	C-2	Ⓕ
Q3012	C-2	Ⓕ
Q3013	C-2	Ⓕ
Q3014	C-2	Ⓕ
Q3015	C-1	Ⓕ
Q3016	B-2	Ⓕ
Q3018	C-2	Ⓕ
Q3019	B-2	Ⓕ
Q3021	B-2	Ⓕ
Q3022	A-2	Ⓕ
Q3023	A-2	Ⓕ
Q3024	A-1	Ⓒ
Q3025	A-2	Ⓕ
Q3027	A-2	Ⓕ
Q3028	A-1	Ⓒ
Q3029	A-1	Ⓕ
Q3201	D-2	Ⓕ
Q3203	D-2	Ⓕ
Q3204	C-2	Ⓕ
Q3206	C-2	Ⓕ
Q3207	C-2	Ⓒ
Q3208	C-2	Ⓕ
Q3209	C-2	Ⓒ
Q3210	C-2	Ⓒ
Q3211	C-2	Ⓒ
Q3212	C-2	Ⓕ
Q3213	C-2	Ⓕ
Q3214	C-2	Ⓕ
Q3215	C-2	Ⓕ
Q3216	B-2	Ⓕ
Q3218	C-2	Ⓕ
Q3219	B-2	Ⓕ
Q3221	B-2	Ⓕ
Q3222	A-2	Ⓕ
Q3223	A-2	Ⓒ
Q3224	A-2	Ⓒ
Q3225	A-2	Ⓕ
Q3227	A-2	Ⓕ
Q3228	A-2	Ⓒ
Q3229	A-2	Ⓕ
Q3401	D-3	Ⓕ
Q3403	D-3	Ⓕ
Q3404	C-3	Ⓕ
Q3406	C-3	Ⓕ
Q3407	C-3	Ⓒ
Q3408	C-3	Ⓕ
Q3409	C-3	Ⓒ
Q3410	C-3	Ⓒ
Q3411	C-3	Ⓒ
Q3412	C-3	Ⓕ
Q3413	C-3	Ⓕ
Q3414	C-3	Ⓕ
Q3415	C-3	Ⓕ
Q3416	B-3	Ⓕ
Q3418	C-3	Ⓕ
Q3419	B-3	Ⓕ
Q3421	B-3	Ⓕ
Q3422	A-3	Ⓕ
Q3423	A-3	Ⓒ
Q3424	A-3	Ⓒ
Q3425	A-3	Ⓕ
Q3427	A-3	Ⓕ
Q3428	A-3	Ⓒ
Q3429	A-3	Ⓕ
Q3601	D-1	Ⓕ
Q3602	C-1	Ⓕ
Q3603	A-1	Ⓕ
Q3604	A-1	Ⓕ
Q3605	C-1	Ⓕ
Integrated Circuit		
IC3001	D-2	Ⓕ
IC3002	C-1	Ⓕ
IC3003	C-1	Ⓒ
IC3004	B-2	Ⓒ
IC3005	A-2	Ⓕ
IC3006	A-2	Ⓒ
IC3201	D-2	Ⓕ
IC3202	C-2	Ⓕ
IC3203	C-2	Ⓒ
IC3204	B-2	Ⓒ
IC3205	A-2	
IC3206	A-3	Ⓒ
IC3401	D-3	Ⓕ
IC3402	C-3	Ⓕ
IC3403	C-3	Ⓒ
IC3404	B-3	Ⓒ
IC3405	A-3	Ⓕ
IC3406	A-3	Ⓒ
IC3601	D-1	Ⓕ
IC3603	C-1	Ⓒ
IC3604	B-1	Ⓕ
IC3605	B-1	Ⓕ
IC3606	A-1	Ⓕ
IC3607	C-1	Ⓕ
IC3608	A-1	Ⓒ
IC3609	C-1	Ⓒ
Test Points		
TP3002	B-2	Ⓕ
TP3003	A-1	Ⓕ
TP3202	B-3	Ⓕ
TP3203	A-2	Ⓕ
TP3402	B-3	Ⓕ
TP3403	A-2	Ⓕ
TG3001	A-1	Ⓕ
Adjustments		
VR3001	A-1	Ⓕ
VR3002	A-1	Ⓕ
VR3003	A-1	Ⓕ
VR3004	B-1	Ⓕ
VR3201	A-2	Ⓕ
VR3202	A-2	Ⓕ
VR3204	B-2	Ⓕ
VR3401	A-3	Ⓕ
VR3402	A-3	Ⓕ
VR3403	A-3	Ⓕ
VR3404	B-3	Ⓕ
Connectors		
P1	C-3	Ⓒ
P2	A-1	Ⓒ
P3	C-1	Ⓒ

ADDRESS INFORMATION
Ⓒ ... COMPONENT SIDE
Ⓕ ... FOIL SIDE

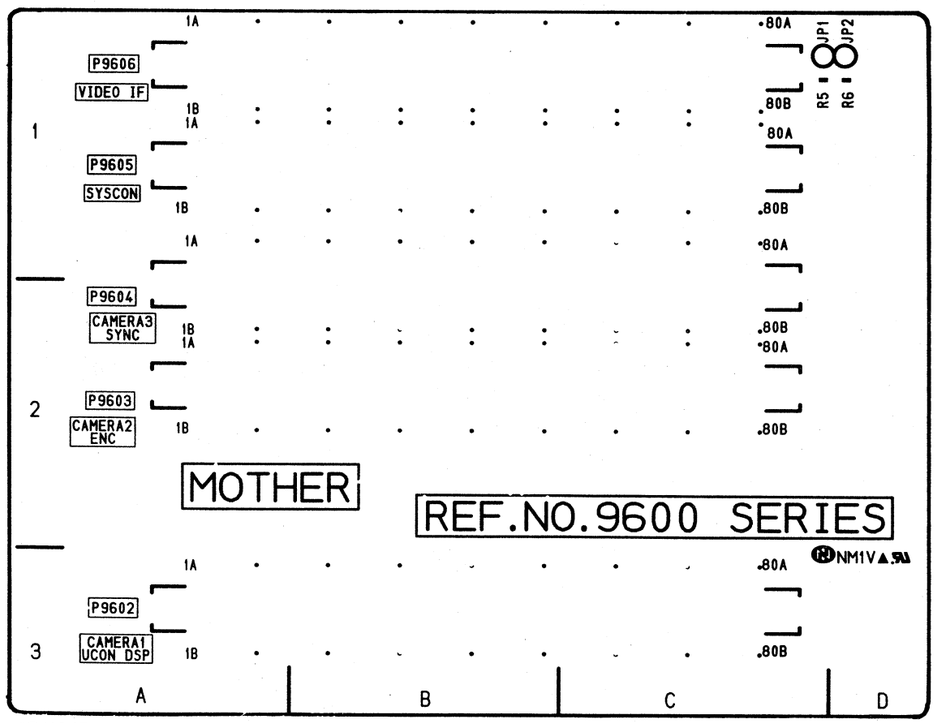
MOTHER P.C. BOARD (VEP00V89A)

MOTHER	
Connectors	
P9601	A-3 Ⓕ
P9602	A-3 Ⓒ
P9603	A-2 Ⓒ
P9604	A-2 Ⓒ
P9605	A-1 Ⓒ
P9606	A-1 Ⓒ
P9607	A-3 Ⓕ
P9608	C-3 Ⓕ
P9610	A-2 Ⓕ
P9611	A-1 Ⓕ
P9612	A-1 Ⓕ
P9613	B-2 Ⓕ
P9614	C-1 Ⓕ
P9617	B-2 Ⓕ
P9619	C-1 Ⓕ
P9620	C-2 Ⓕ
P9621	C-1 Ⓕ
P9622	A-1 Ⓕ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE



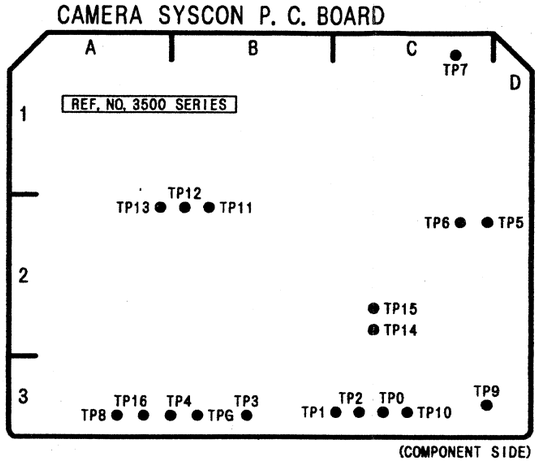
(FOIL SIDE)



(COMPONENT SIDE)

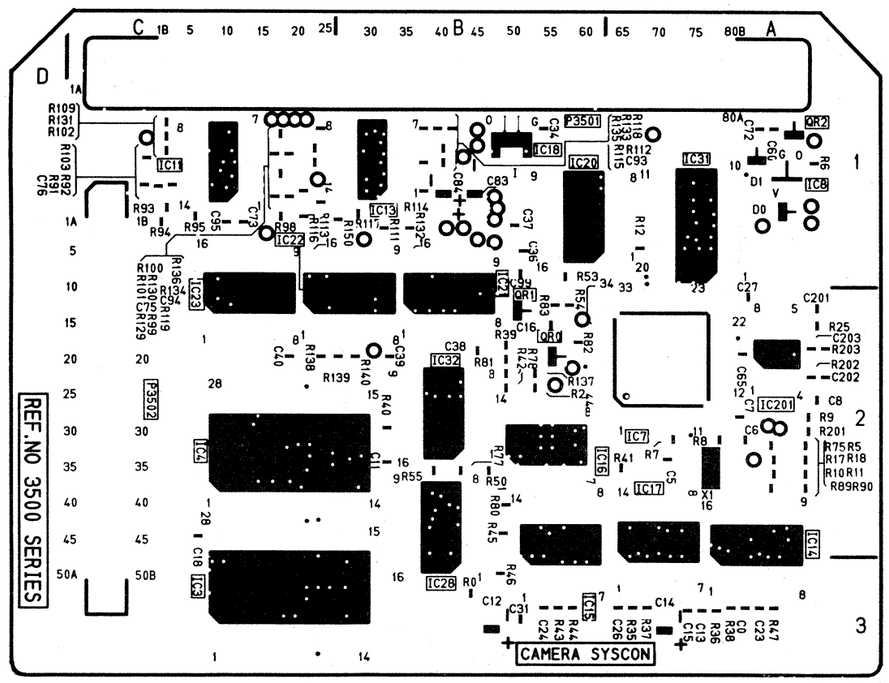
3—4

CAMERA SYSCON P.C. BOARD (VEP26074A)



CAMERA SYSCON		
Transistors		
Q3500	C-1	©
Q3501	C-1	©
Q3502	C-1	©
Q3503	B-1	©
Q3504	B-1	©
Q3505	C-1	©
Transistor-Resistors		
QR3500	B-2	Ⓕ
QR3501	B-2	Ⓕ
QR3502	A-1	Ⓕ
QR3503	B-2	©
Integrated Circuits		
IC3201	A-2	Ⓕ
IC3501	B-2	©
IC3502	B-3	©
IC3503	C-3	Ⓕ
IC3504	C-2	Ⓕ
IC3505	C-3	©
IC3506	B-2	©
IC3507	A-2	Ⓕ
IC3508	A-1	Ⓕ
IC3510	C-1	©
IC3511	C-1	Ⓕ
IC3513	B-1	Ⓕ
IC3514	A-2	Ⓕ
IC3515	B-3	Ⓕ
IC3516	B-2	Ⓕ
IC3517	A-2	Ⓕ
IC3518	B-1	Ⓕ
IC3519	B-2	©
IC3520	B-1	Ⓕ
IC3521	B-2	Ⓕ
IC3522	B-1	Ⓕ
IC3523	C-2	Ⓕ
IC3525	B-1	©
IC3526	C-2	©
IC3528	B-3	Ⓕ
IC3529	B-2	©
IC3530	A-1	©
IC3531	A-1	Ⓕ
IC3532	B-2	Ⓕ
IC3533	C-2	©
Test Points		
TP3500	C-3	©
TP3501	B-3	©
TP3502		
TP3503	B-3	©
TP3504	A-3	©
TP3505	C-2	©
TP3506	C-2	©
TP3507	C-1	©
TP3508	A-3	©
TP3509	C-3	©
TP3510	C-3	©
TP3511	B-2	©
TP3512	B-2	©
TP3513	A-2	©
TP3514	C-2	©
TP3515	C-2	©
TP3516	A-3	©
TG3500	B-3	©
Connectors		
P3501	B-1	Ⓕ
P3502	C-2	Ⓕ
P3503	C-3	©

ADDRESS INFORMATION
©...COMPONENT SIDE
Ⓕ...FOIL SIDE



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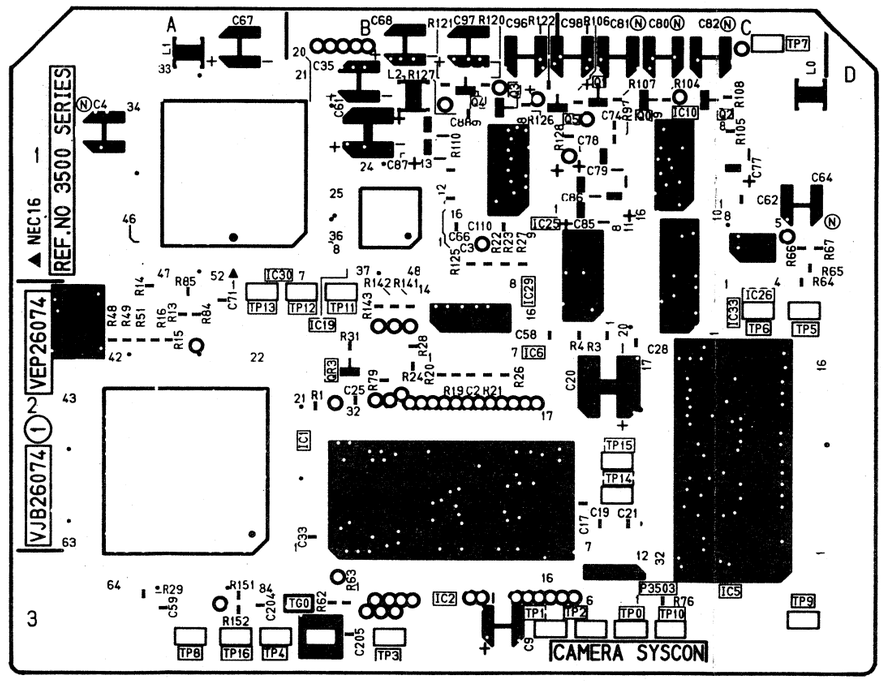
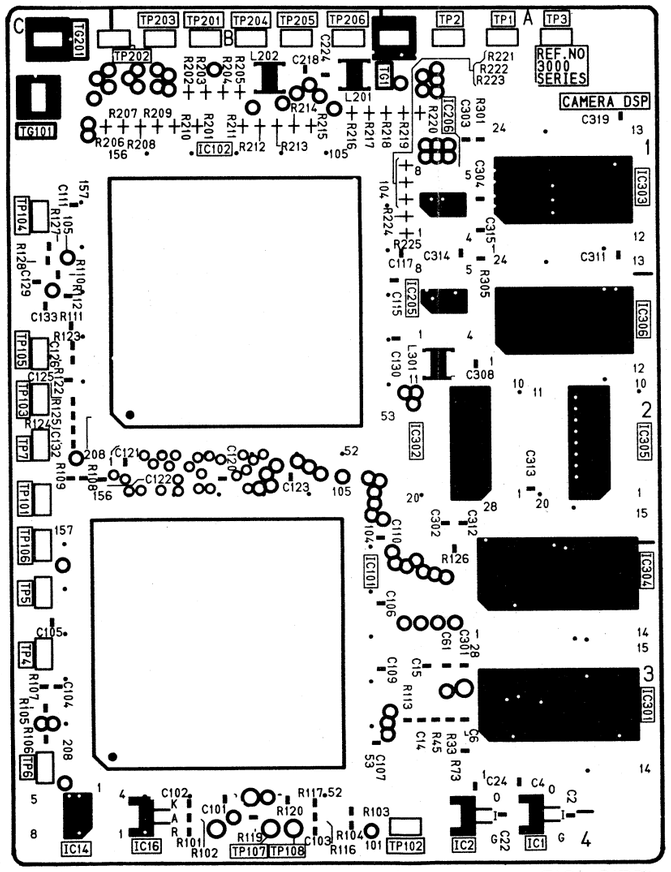


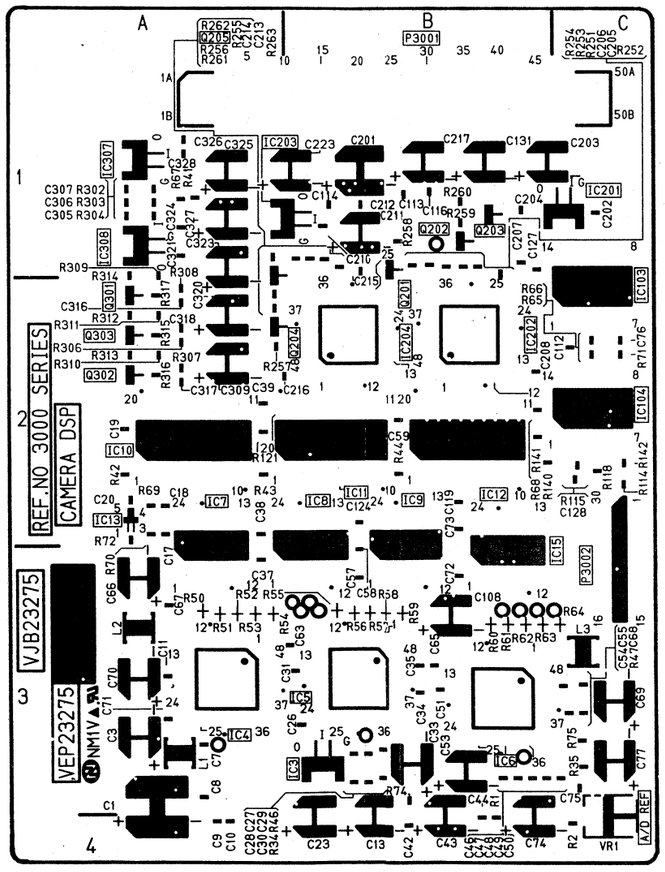
(COMPONENT SIDE)

3—5

CAMERA DSP P.C. BOARD (VEP23275A)



(FIOL SIDE)

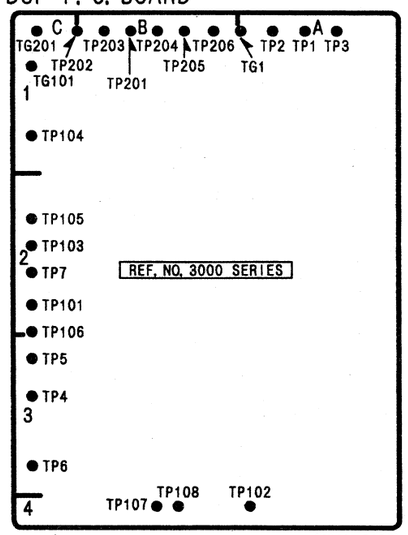


(COMPONENT SIDE)

CAMERA DSP					
Transistors			IC3305	A-2	Ⓕ
Q3201	B-2	Ⓒ	IC3306	A-2	Ⓕ
Q3202	B-1	Ⓒ	IC3307	A-1	Ⓒ
Q3203	B-1	Ⓒ	IC3308	A-1	Ⓒ
Q3204	B-2	Ⓒ	**Test Points**		
Q3205	A-1	Ⓒ	TP3001	A-1	Ⓕ
Integrated Circuits			TP3002	A-1	Ⓕ
IC3001	A-4	Ⓕ	TP3003	A-1	Ⓕ
IC3002	A-4	Ⓕ	TP3004	C-3	Ⓕ
IC3003	B-3	Ⓒ	TP3005	C-3	Ⓕ
IC3004	A-3	Ⓒ	TP3006	C-3	Ⓕ
IC3005	B-3	Ⓒ	TP3007	C-2	Ⓕ
IC3006	B-3	Ⓒ	TP3101	C-2	Ⓕ
IC3007	A-2	Ⓒ	TP3102	A-4	Ⓕ
IC3008	B-2	Ⓒ	TP3103	C-3	Ⓕ
IC3009	B-2	Ⓒ	TP3104	C-1	Ⓕ
IC3010	A-2	Ⓒ	TP3105	C-2	Ⓕ
IC3011	B-2	Ⓒ	TP3106	B-4	Ⓕ
IC3012	B-2	Ⓒ	TP3107	C-3	Ⓕ
IC3013	A-2	Ⓒ	TP3108	B-4	Ⓕ
IC3014	C-4	Ⓕ	TP3201	B-1	Ⓕ
IC3015	C-2	Ⓒ	TP3202	B-1	Ⓕ
IC3016	B-4	Ⓕ	TP3203	B-1	Ⓕ
IC3101	B-3	Ⓕ	TP3204	B-1	Ⓕ
IC3102	B-1	Ⓕ	TP3205	B-1	Ⓕ
IC3103	C-2	Ⓒ	TP3206	B-1	Ⓕ
IC3104	C-2	Ⓒ	TG3001	A-1	Ⓕ
IC3201	C-1	Ⓒ	TG3101	C-1	Ⓕ
IC3202	B-2	Ⓒ	TG3201	C-1	Ⓕ
IC3203	B-1	Ⓒ	**Adjustments**		
IC3204	B-2	Ⓒ	VR3001	C-4	Ⓒ
IC3205	A-2	Ⓕ	**Connectors**		
IC3206	A-1	Ⓕ	P3001	B-1	Ⓒ
IC3301	A-3	Ⓕ	P3002	C-3	Ⓒ
IC3302	A-2	Ⓕ			
IC3303	A-1	Ⓕ			
IC3304	A-3	Ⓕ			

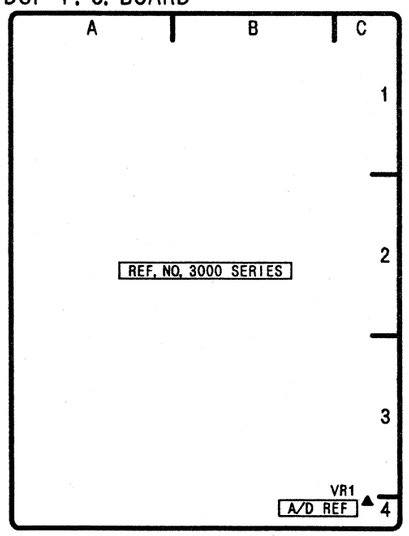
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

DSP P. C. BOARD



(FOIL SIDE)

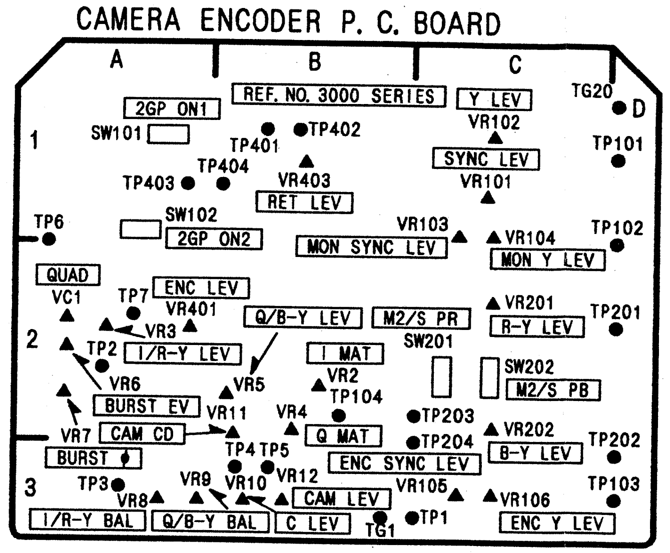
DSP P. C. BOARD



(COMPONENT SIDE)

3—6

CAMERA ENCODER P.C. BOARD (VEP23276A)



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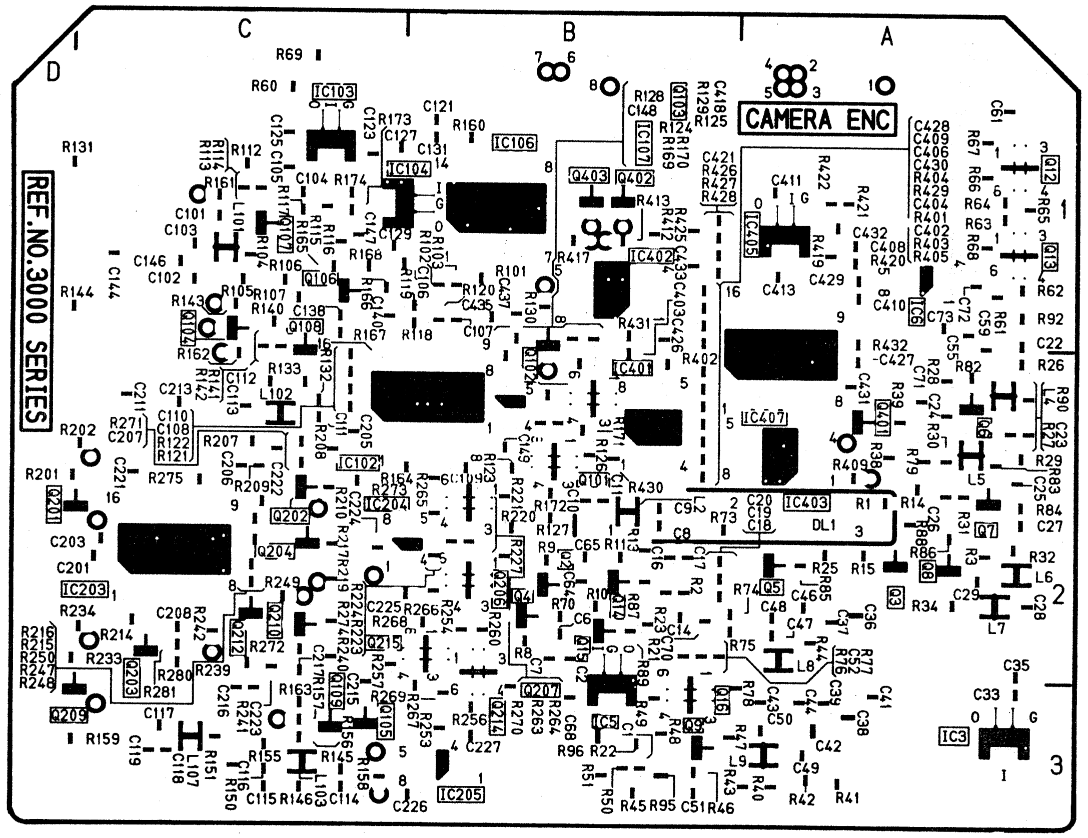

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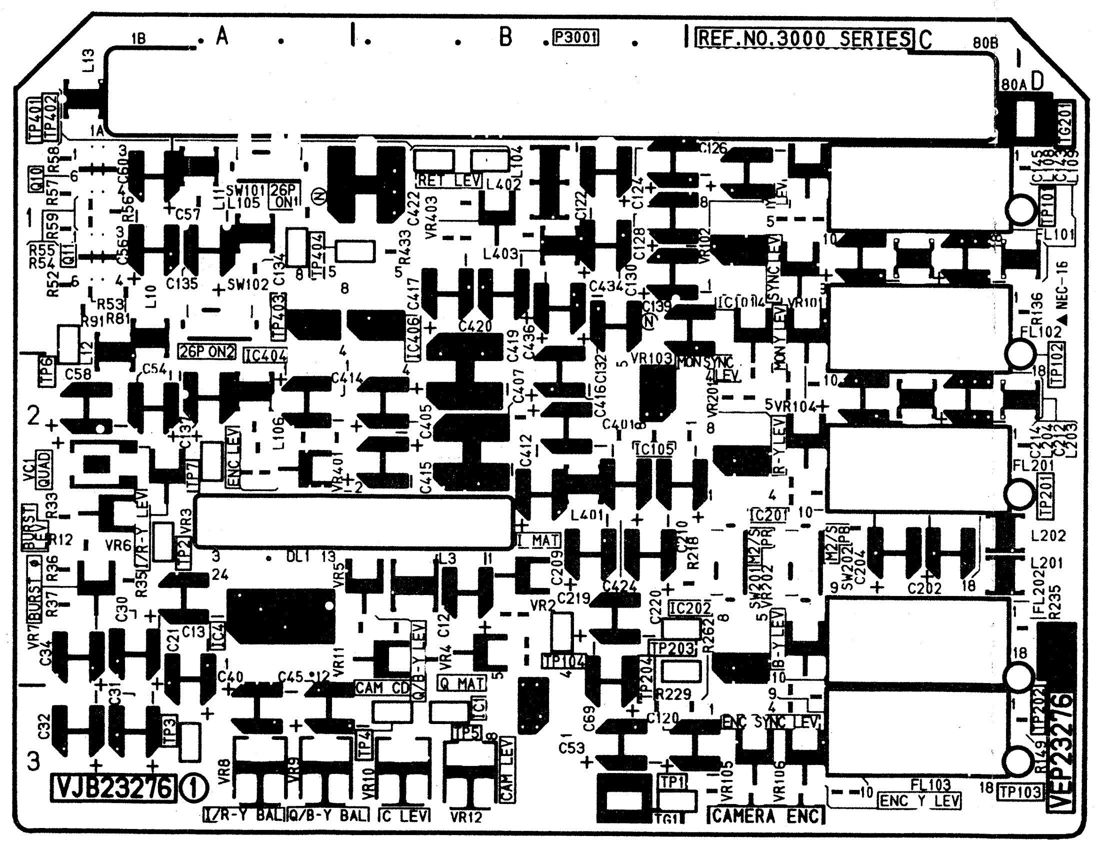


(COMPONENT SIDE)

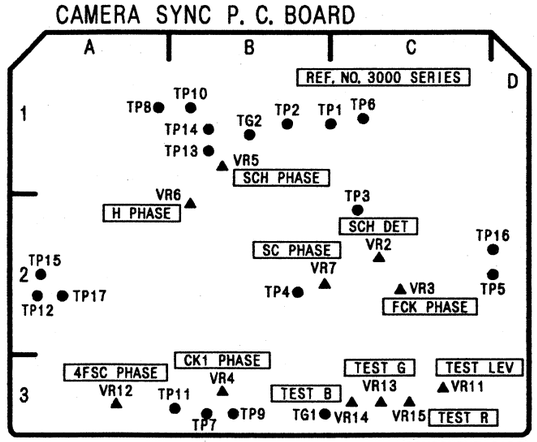
CAMERA ENCODER

Part	Address	Side
Transistors		
Q3003	A-2	Ⓕ
Q3005	A-2	Ⓕ
Q3006	A-2	Ⓕ
Q3008	A-2	Ⓕ
Q3009	B-3	Ⓕ
Q3010	A-1	Ⓒ
Q3011	A-1	Ⓒ
Q3012	A-1	Ⓕ
Q3013	A-1	Ⓕ
Q3014	B-2	Ⓕ
Q3015	B-2	Ⓕ
Q3016	B-3	Ⓕ
Q3101	B-2	Ⓕ
Q3102	B-2	Ⓕ
Q3103	B-1	Ⓕ
Q3104	C-1	Ⓕ
Q3105	C-3	Ⓕ
Q3106	C-1	Ⓕ
Q3107	C-1	Ⓕ
Q3108	C-1	Ⓕ
Q3109	C-3	Ⓕ
Q3201	D-2	Ⓕ
Q3202	C-2	Ⓕ
Q3203	C-3	Ⓒ
Q3204	C-2	Ⓕ
Q3206	B-2	Ⓕ
Q3207	B-3	Ⓕ
Q3209	D-3	Ⓕ
Q3210	C-2	Ⓕ
Q3212	C-2	Ⓕ
Q3214	B-3	Ⓕ
Q3215	C-2	Ⓕ
Q3401	A-2	Ⓕ
Q3402	B-1	Ⓕ
Q3403	B-1	Ⓕ
Integrated Circuits		
IC3001	B-3	Ⓒ
IC3003	A-3	Ⓕ
IC3004	A-2	Ⓒ
IC3005	B-3	Ⓕ
IC3006	A-1	Ⓕ
IC3101	C-1	Ⓒ
IC3102	C-2	Ⓕ
IC3103	C-1	Ⓕ
IC3104	C-1	Ⓕ
IC3105	B-2	Ⓒ
IC3106	B-1	Ⓕ
IC3107	B-1	Ⓕ
IC3201	C-2	Ⓒ
IC3202	B-2	Ⓒ
IC3203	C-2	Ⓕ
IC3204	C-2	Ⓕ
IC3205	B-3	Ⓕ
IC3401	B-2	Ⓕ
IC3402	B-1	Ⓕ
IC3403	A-2	Ⓕ
IC3404	A-1	Ⓒ
IC3405	A-1	Ⓕ
IC3406	B-1	Ⓒ
Test Points		
TP3001	B-3	Ⓒ
TP3002	A-2	Ⓒ
TP3003	A-3	Ⓒ
TP3004	B-3	Ⓒ
TP3005	B-3	Ⓒ
TP3006	A-2	Ⓒ
TP3007	A-2	Ⓒ
TP3101	A-2	Ⓒ
TP3102	A-3	Ⓒ
TP3103	D-3	Ⓒ
TP3104	B-2	Ⓒ
TP3105	D-1	Ⓒ
TP3106	A-2	Ⓒ
TP3201	D-2	Ⓒ
TP3202	D-3	Ⓒ
TP3203	B-2	Ⓒ
TP3401	A-1	Ⓒ
TP3402	A-1	Ⓒ
TP3403	A-1	Ⓒ
TP3404	A-1	Ⓒ
TG3001	B-3	Ⓒ
TG3201	D-1	Ⓒ
Adjustments		
VC3001	A-2	Ⓒ
VR3003	A-2	Ⓒ
VR3005	A-2	Ⓒ
VR3006	A-2	Ⓒ
VR3008	A-3	Ⓒ
VR3009	A-3	Ⓒ
VR3010	B-3	Ⓒ
VR3011	A-2	Ⓒ
VR3012	B-3	Ⓒ
VR3101	C-1	Ⓒ
VR3102	A-2	Ⓒ
VR3103	B-1	Ⓒ
VR3104	B-2	Ⓒ
VR3105	C-3	Ⓒ
VR3106	C-3	Ⓒ
VR3201	C-2	Ⓒ
VR3202	C-2	Ⓒ
VR3401	A-2	Ⓒ
VR3403	B-1	Ⓒ
Switches		
SW3101	A-1	Ⓒ
SW3102	A-1	Ⓒ
SW3201	C-2	Ⓒ
SW3202	C-2	Ⓒ
Connectors		
P3001	B-1	Ⓒ

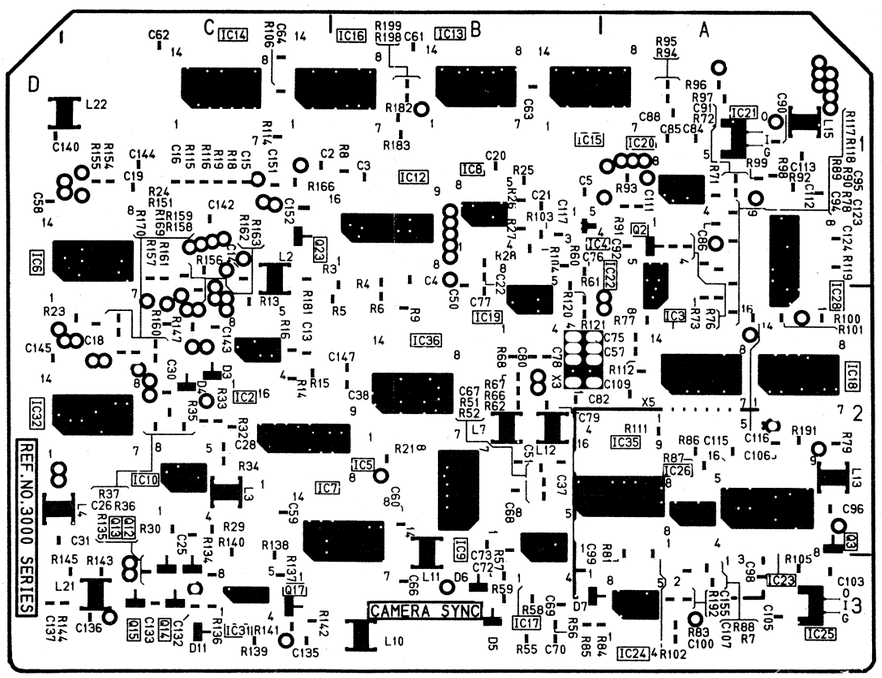
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

3—7

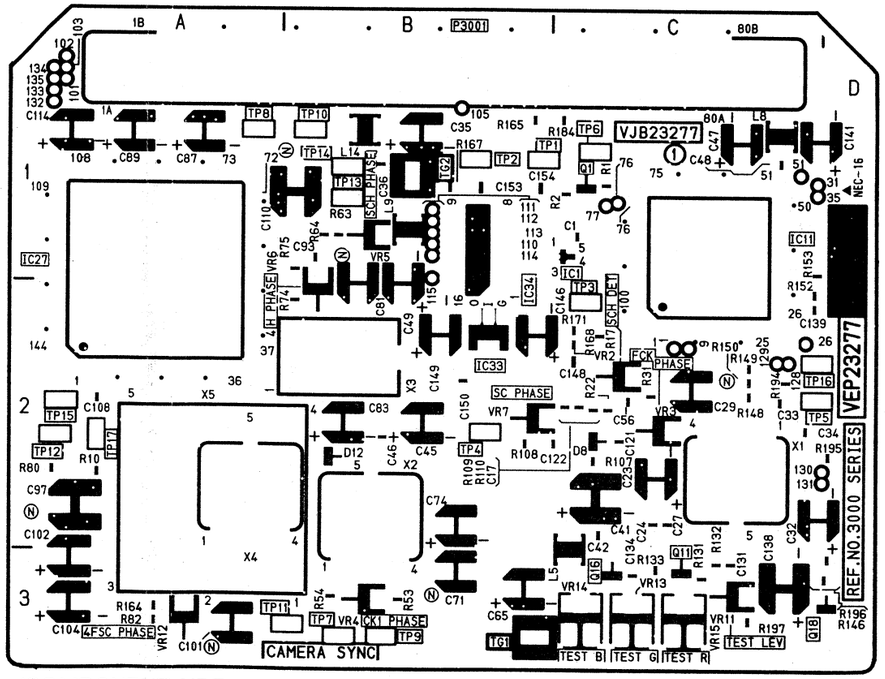
CAMERA SYNC P.C. BOARD (VEP23277A)



(COMPONENT SIDE)



(FIOL SIDE)



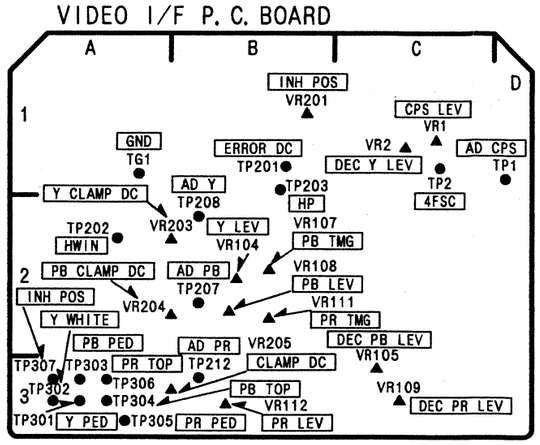
(COMPONENT SIDE)

CAMERA SYNC					
Transistors			IC3033	B-2	©
Q3001	C-1	©	IC3034	B-1	©
Q3002	A-1	Ⓕ	IC3035	A-2	Ⓕ
Q3003	A-2	Ⓕ	IC3036	B-2	Ⓕ
Q3011	C-1	©	**Test Points**		
Q3012	C-2	Ⓕ	TP3001	B-1	©
Q3013	C-2	Ⓕ	TP3002	B-1	©
Q3014	C-3	Ⓕ	TP3003	C-1	©
Q3015	C-3	Ⓕ	TP3004	B-2	©
Q3016	C-3	©	TP3005	C-2	©
Q3017	C-3	Ⓕ	TP3006	C-1	©
Q3018	C-3	©	TP3007	B-3	©
Q3023	C-1	Ⓕ	TP3008	A-1	©
Integrated Circuits			TP3009	B-3	©
IC3002	C-2	Ⓕ	TP3010	B-2	©
IC3003	A-2	Ⓕ	TP3011	A-3	©
IC3005	B-2	Ⓕ	TP3012	A-2	©
IC3006	D-1	Ⓕ	TP3013	B-2	©
IC3007	C-2	Ⓕ	TP3014	B-2	©
IC3008	B-1	Ⓕ	TP3015	A-2	©
IC3009	B-3	Ⓕ	TP3016	C-2	©
IC3010	C-2	Ⓕ	TP3017	A-2	©
IC3011	C-2	©	TG3001	B-3	©
IC3013	B-1	Ⓕ	TG3002	B-2	©
IC3014	C-1	Ⓕ	**Adjustments**		
IC3015	B-1	Ⓕ	VR3002	C-2	©
IC3016	B-1	Ⓕ	VR3005	B-1	©
IC3017	B-3	Ⓕ	VR3006	A-1	©
IC3018	A-2	Ⓕ	VR3007	B-2	©
IC3019	B-2	Ⓕ	VR3011	C-3	©
IC3020	A-1	Ⓕ	VR3012	A-3	©
IC3021	A-1	Ⓕ	VR3013	C-3	©
IC3022	A-1	Ⓕ	VR3014	C-3	©
IC3023	A-3	Ⓕ	VR3015	C-3	©
IC3024	A-3	Ⓕ	**Connectors**		
IC3025	A-3	Ⓕ	P3001	B-1	©
IC3027	A-1	©			
IC3028	A-2	Ⓕ			
IC3031	C-3	Ⓕ			
IC3032	D-2	Ⓕ			

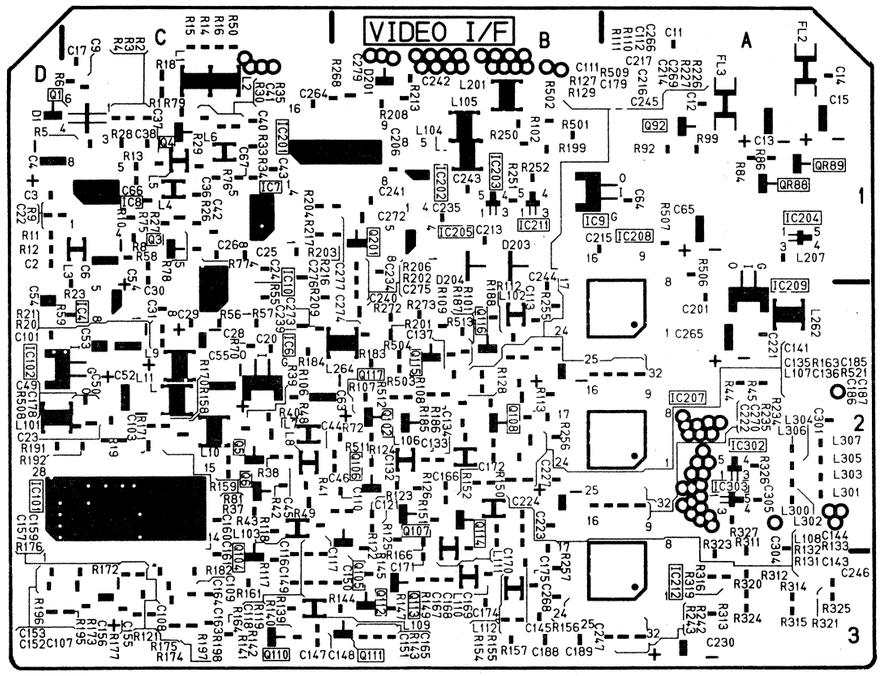
ADDRESS INFORMATION
© ... COMPONENT SIDE
Ⓕ ... FOIL SIDE

3—8

VIDEO I/F P.C. BOARD (VEP03B94A)



(COMPONENT SIDE)



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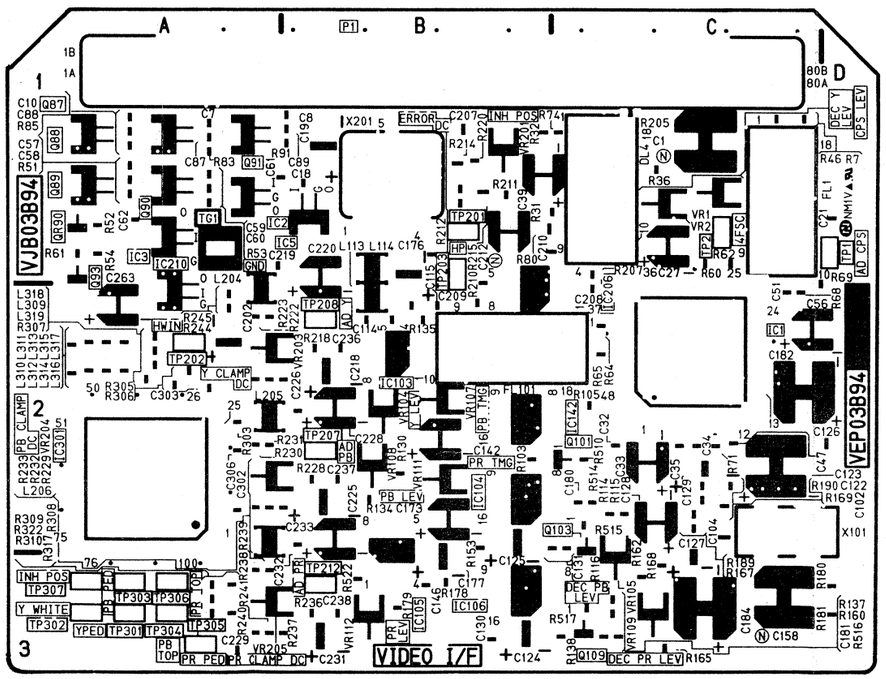


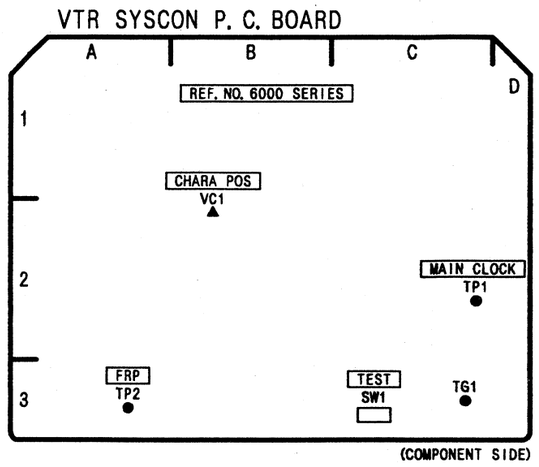
(COMPONENT SIDE)

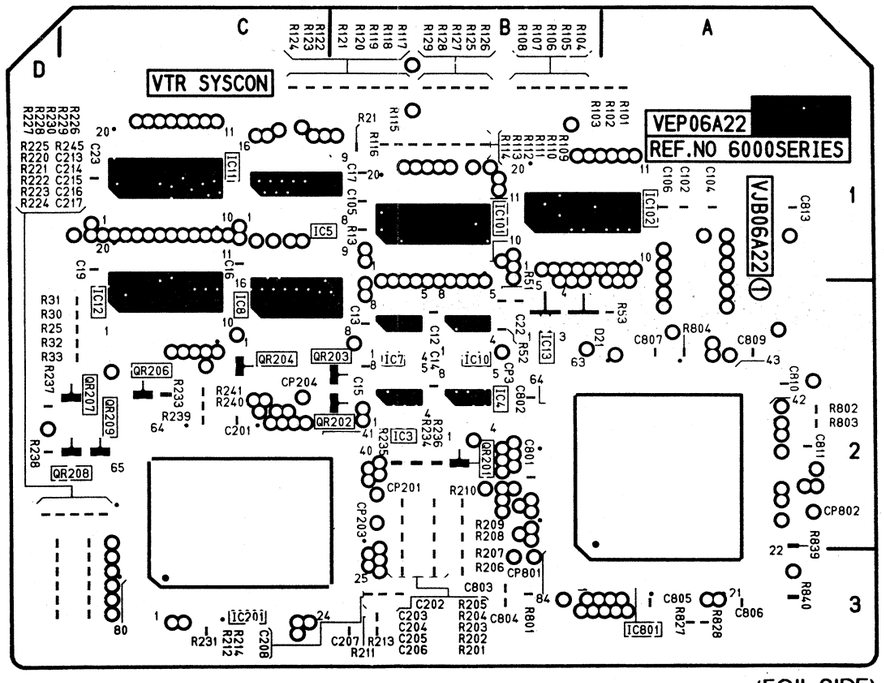
VIDEO I/F				
Transistors			IC104	C-3 Ⓕ
Q1	D-1 Ⓕ		IC105	B-3 Ⓒ
Q3	C-1 Ⓕ		IC106	B-3 Ⓒ
Q4	C-1 Ⓕ		IC142	
Q5	C-2 Ⓕ		IC201	C-1 Ⓕ
Q6	C-2 Ⓕ		IC202	B-1 Ⓕ
Q7			IC203	B-1 Ⓕ
Q8			IC204	A-1 Ⓕ
Q9			IC205	B-1 Ⓕ
Q87	A-1 Ⓒ		IC206	
Q88	A-1 Ⓒ		IC207	A-2 Ⓕ
Q89	A-1 Ⓒ		IC208	A-1 Ⓕ
Q90	A-1 Ⓒ		IC209	A-2 Ⓕ
Q91	A-1 Ⓒ		IC211	B-1 Ⓕ
Q92	A-1 Ⓒ		IC212	A-3 Ⓕ
Q93	A-1 Ⓒ		IC301	A-2 Ⓒ
Q101	C-2 Ⓒ		**Test Points**	
Q102	B-2 Ⓕ		TP1	D-1 Ⓒ
Q103	C-2 Ⓒ		TP2	C-1 Ⓒ
Q104	B-2 Ⓒ		TP201	B-1 Ⓒ
Q105	B-3 Ⓕ		TP202	A-2 Ⓒ
Q106	B-2 Ⓕ		TP203	B-1 Ⓒ
Q107	B-2 Ⓕ		TP207	B-2 Ⓒ
Q108	B-2 Ⓕ		TP208	B-2 Ⓒ
Q109	C-3 Ⓒ		TP212	B-3 Ⓒ
Q110	C-3 Ⓕ		TP301	A-3 Ⓒ
Q111	B-3 Ⓕ		TP302	A-3 Ⓒ
Q112	B-3 Ⓕ		TP303	A-3 Ⓒ
Q113	B-3 Ⓕ		TP304	A-3 Ⓒ
Q114	B-2 Ⓕ		TP305	A-3 Ⓒ
Q115	B-2 Ⓕ		TP306	A-3 Ⓒ
Q116	B-2 Ⓕ		TP307	A-3 Ⓒ
Q201	B-1 Ⓕ		TG1	A-1 Ⓒ
Transistor-Resistors			**Adjustments**	
QR88	A-1 Ⓕ		VR1	C-1 Ⓒ
QR89	A-1 Ⓕ		VR2	C-1 Ⓒ
QR90	A-1 Ⓒ		VR104	B-2 Ⓒ
Integrated Circuits			VR105	C-3 Ⓒ
IC1	C-2 Ⓒ		VR107	B-2 Ⓒ
IC4	C-2 Ⓕ		VR108	B-2 Ⓒ
IC5	B-1 Ⓒ		VR109	C-3 Ⓒ
IC6	B-2 Ⓕ		VR111	B-2 Ⓒ
IC7	B-1 Ⓕ		VR112	B-3 Ⓒ
IC8	C-1 Ⓕ		VR201	B-1 Ⓒ
IC10	B-2 Ⓕ		**Connectors**	
IC101	D-2 Ⓕ		P1	B-1 Ⓒ
IC102	D-2 Ⓕ			
IC103	B-2 Ⓒ			

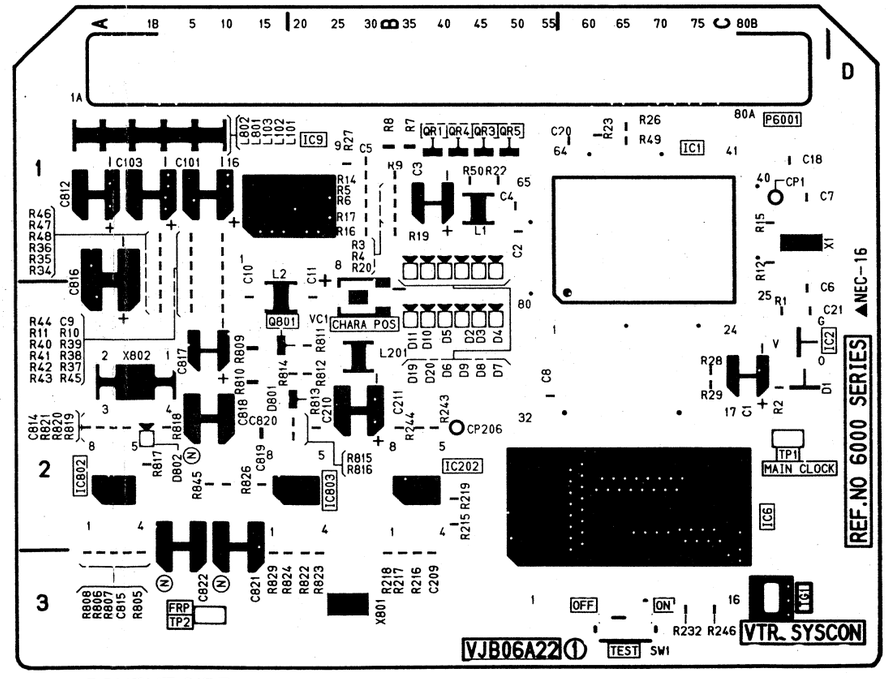
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

3—9

VTR SYSCON P.C. BOARD (VEP06A22A)





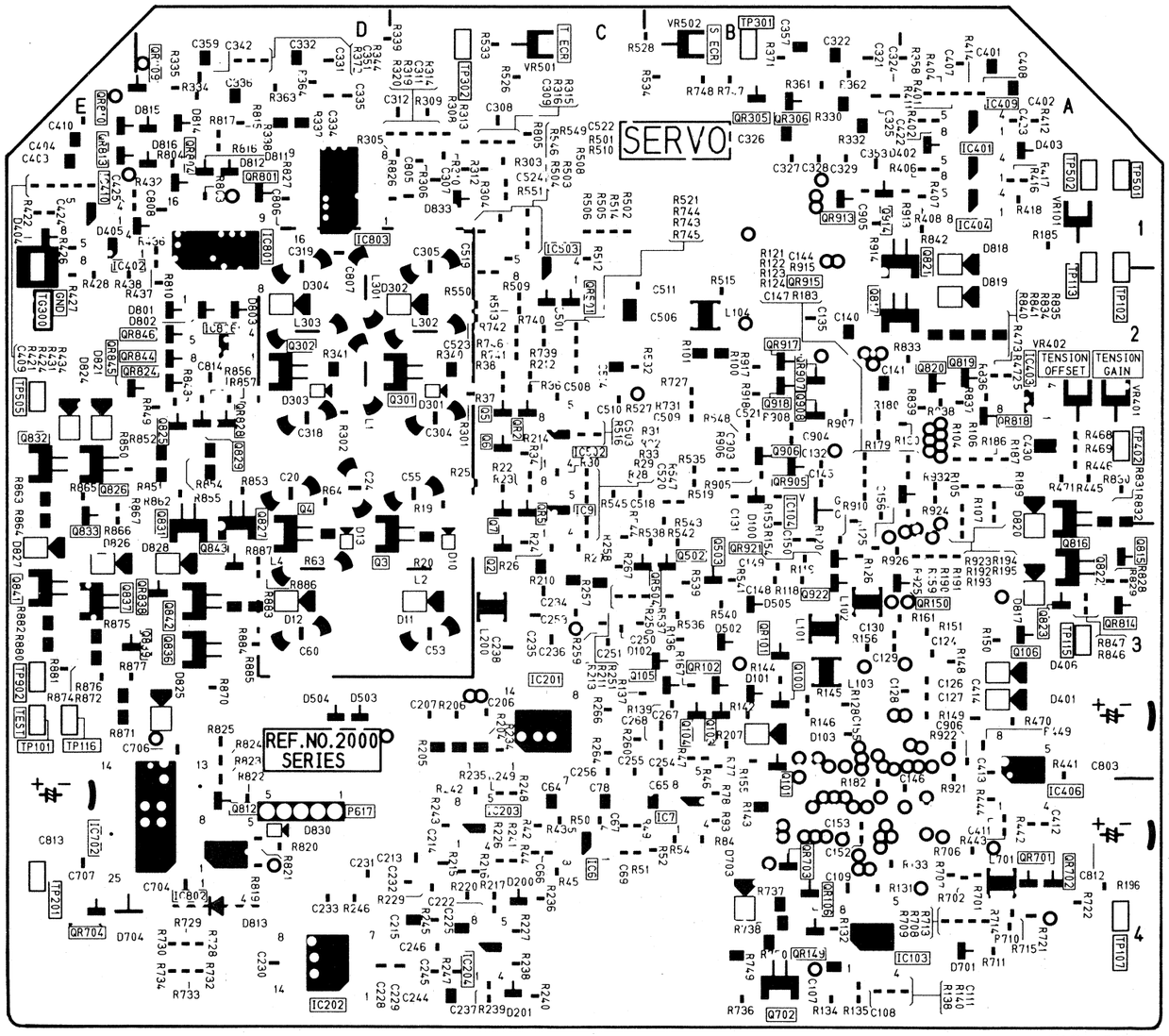


VTR SYSCON		
Transistors		
Q6801	A-2	©
Transistor-Resistors		
QR6001	B-1	©
QR6003	B-1	©
QR6004	B-1	©
QR6005	B-1	©
QR6201	B-2	Ⓕ
QR6202	B-2	Ⓕ
QR6203	B-2	Ⓕ
QR6204	C-2	Ⓕ
QR6206	C-2	Ⓕ
QR6207	C-2	Ⓕ
QR6208	C-2	Ⓕ
QR6209	C-2	Ⓕ
Integrated Circuits		
IC6001	C-1	©
IC6002	D-2	©
IC6003	B-2	Ⓕ
IC6004	B-2	Ⓕ
IC6005	C-1	Ⓕ
IC6006	C-2	©
IC6007	B-2	Ⓕ
IC6008	C-2	Ⓕ
IC6009	B-1	©
IC6010	B-2	Ⓕ
IC6011	C-1	Ⓕ
IC6012	C-2	Ⓕ
IC6013	B-2	Ⓕ
IC6101	B-1	Ⓕ
IC6102	A-1	Ⓕ
IC6201	C-3	Ⓕ
IC6202	B-2	©
IC6801	A-3	Ⓕ
IC6802	B-2	©
IC6803	B-2	©
Test Points		
TP6001	C-2	©
TP6002	A-3	©
TG6001	C-3	©
Adjustments		
VC6001	B-2	©
Switches		
SW6001	C-3	©
Connectors		
P6001	C-1	©

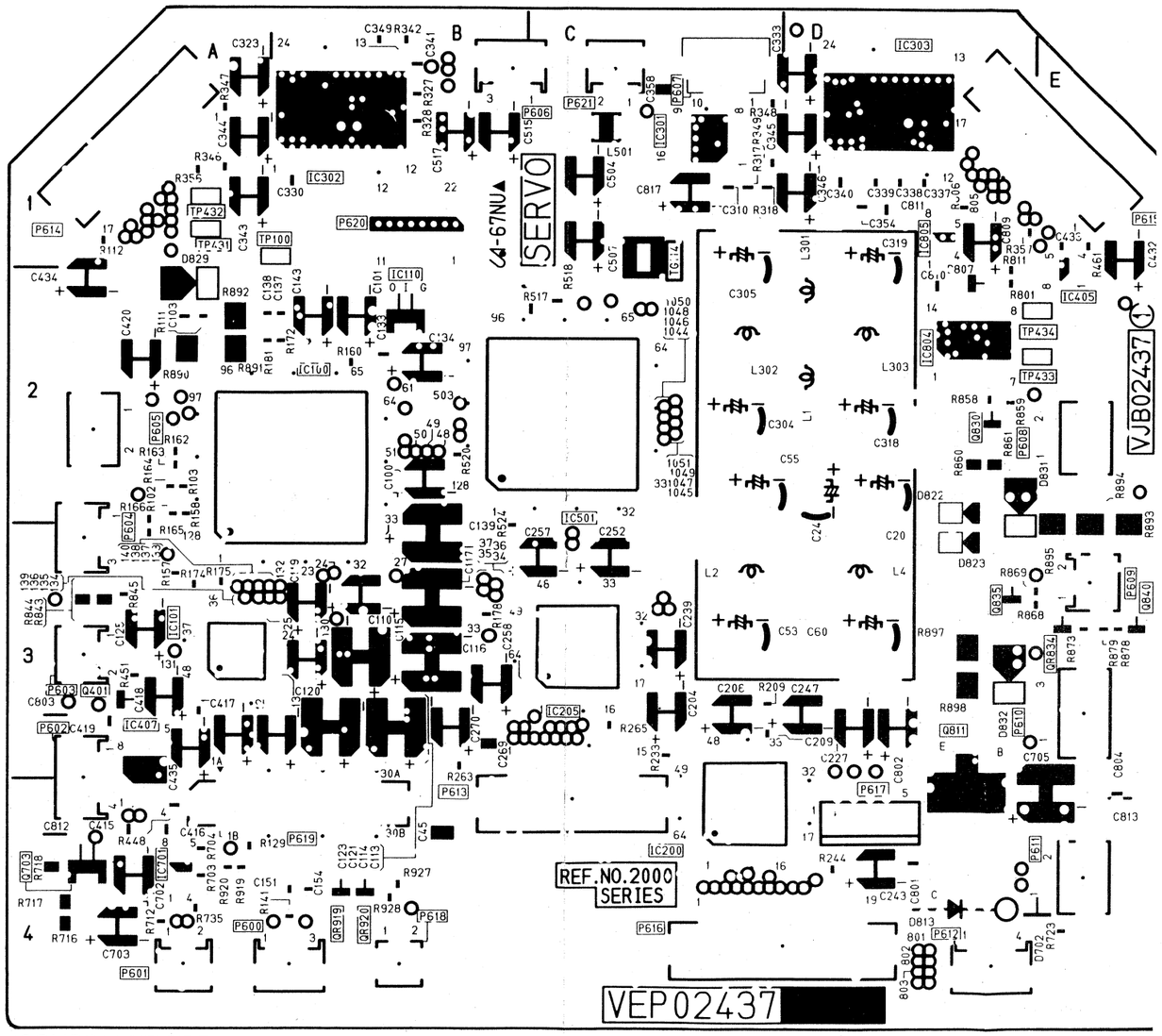
ADDRESS INFORMATION
© ... COMPONENT SIDE
Ⓕ ... FOIL SIDE

3—10

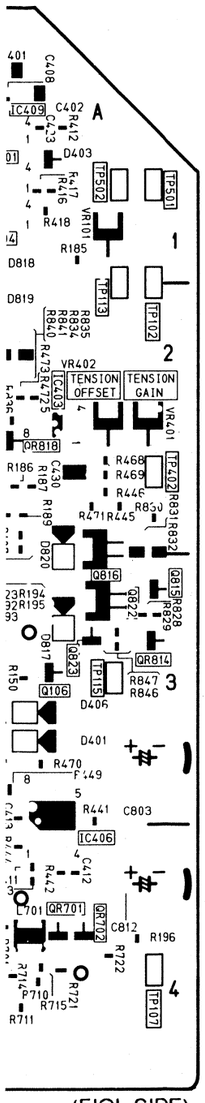
SERVO P.C. BOARD (VEP02437A)



(FIOL SIDE)



(COMPONENT SIDE)



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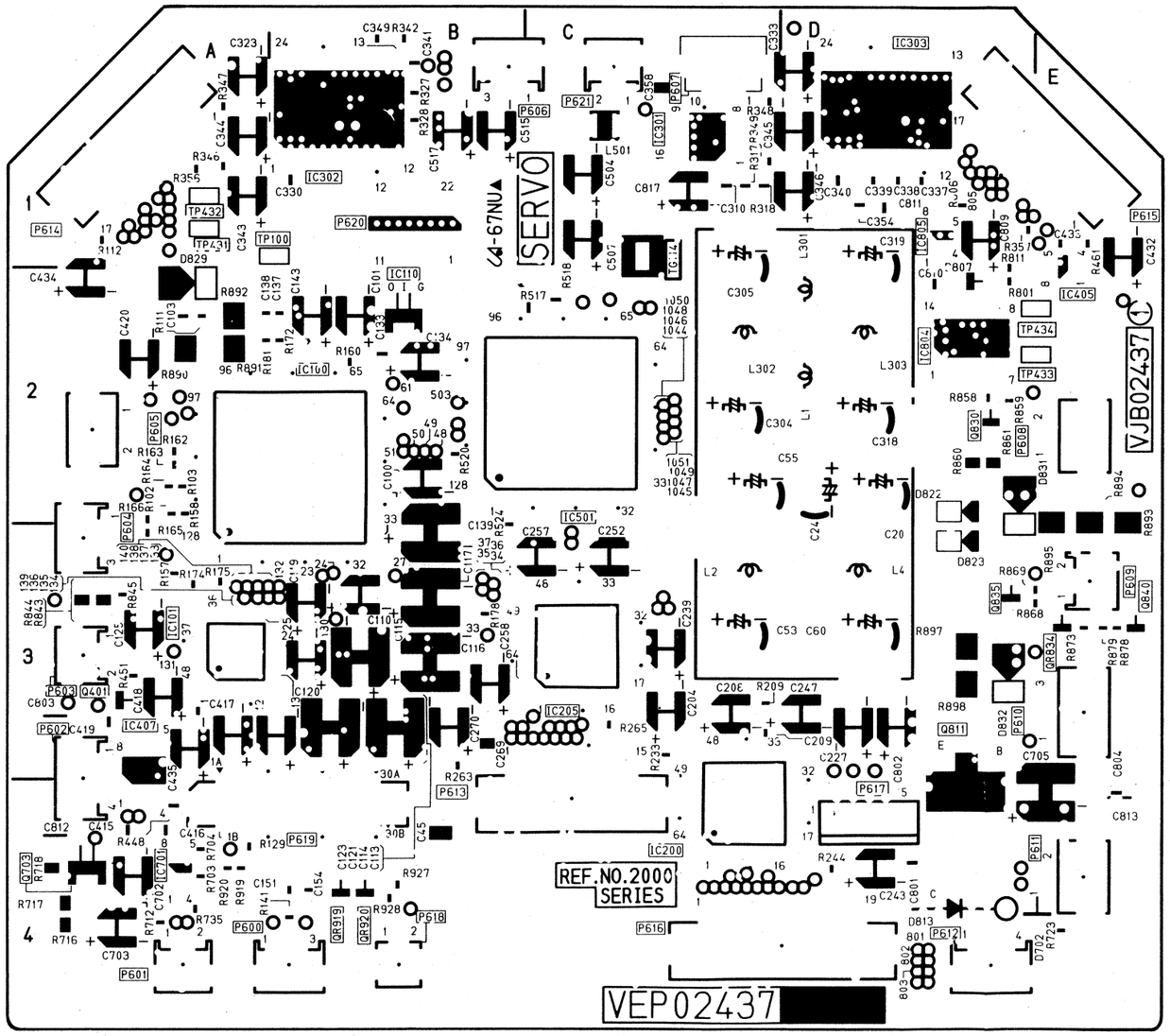
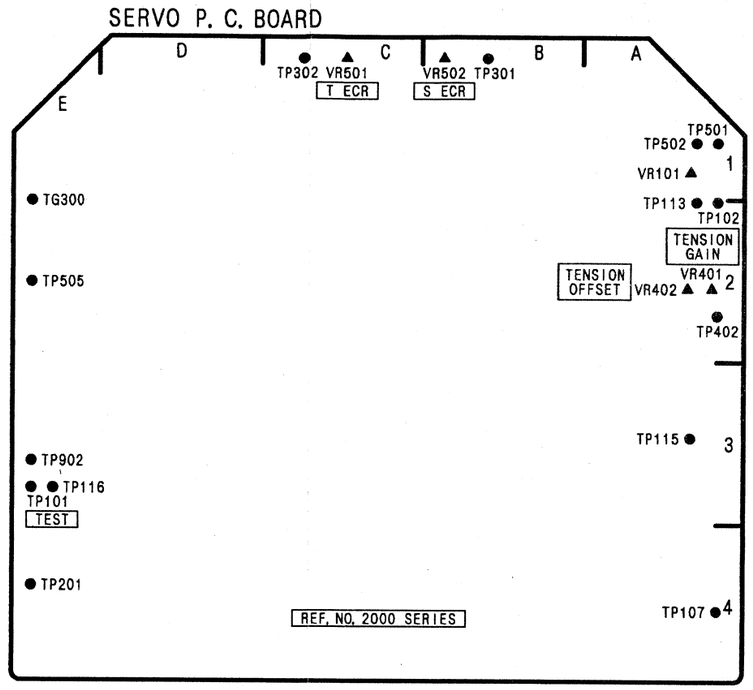


(COMPONENT SIDE)



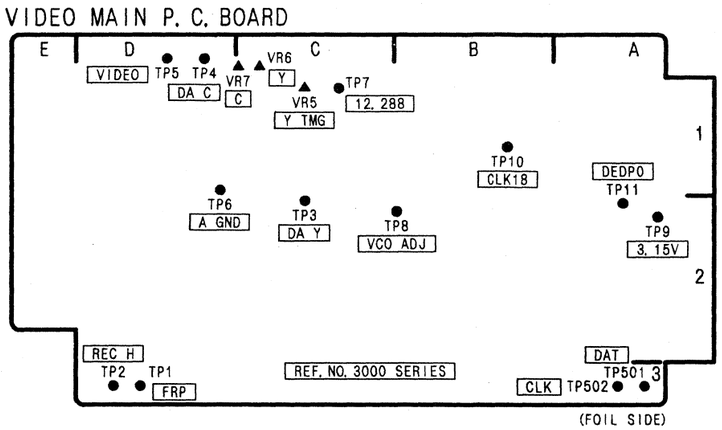
(FOIL SIDE)

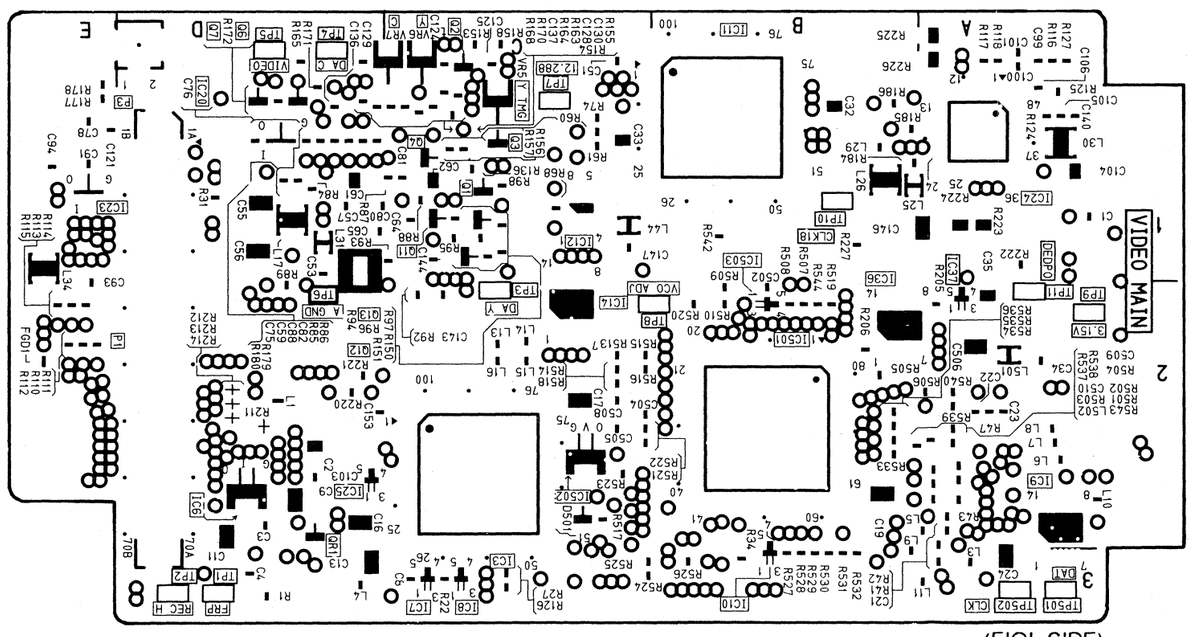
SERVO

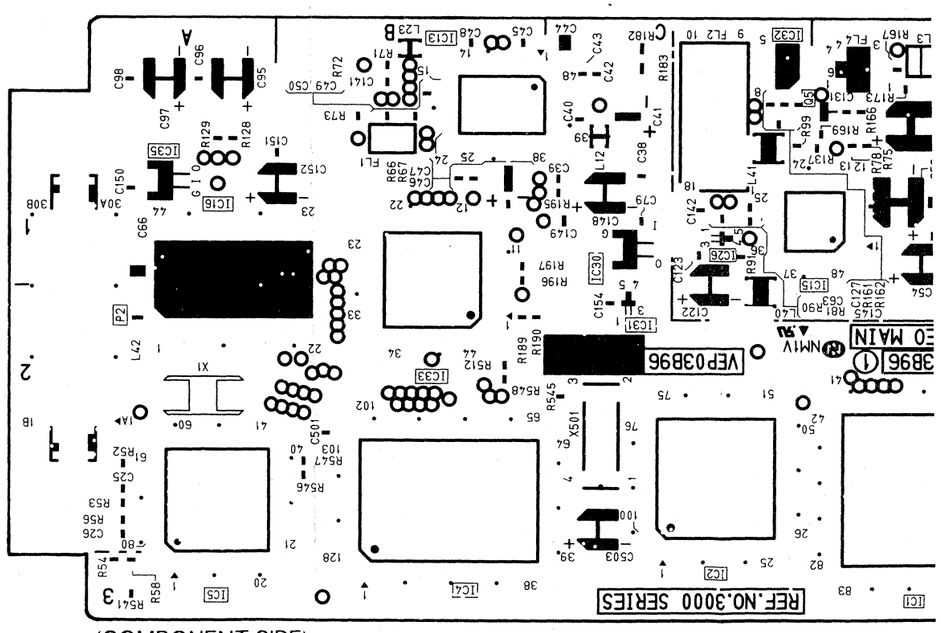
Transistors												
Q2	C-3 Ⓕ	Q906	B-2 Ⓕ	IC101	A-3 Ⓒ	TP431	A-1 Ⓒ	Adjustments				
Q3	D-3 Ⓕ	Q908	B-2 Ⓕ	IC103	A-4 Ⓕ	TP432	A-1 Ⓒ	VR100				
Q4	D-2 Ⓕ	Q914	B-1 Ⓕ	IC104	B-2 Ⓕ	TP433	E-2 Ⓒ	VR101	A-1 Ⓕ			
Q5	C-2 Ⓕ	Q918	B-2 Ⓕ	IC110	B-2 Ⓒ	TP434	E-2 Ⓒ	VR401	A-2 Ⓕ			
Q6	C-2 Ⓕ	Q922	B-3 Ⓕ	IC200	C-4 Ⓒ	TP501	A-1 Ⓕ	VR402	A-2 Ⓕ			
Q7	C-2 Ⓕ	Transistor-Resistors		IC201	C-3 Ⓕ	TP502	A-1 Ⓕ	VR501	C-1 Ⓕ			
Q100	B-3 Ⓕ	QR2	C-2 Ⓕ	IC202	D-4 Ⓕ	TP505	E-2 Ⓕ	VR502	B-1 Ⓕ			
Q101	B-3 Ⓕ	QR5	C-2 Ⓕ	IC203	C-4 Ⓕ	TP902	E-3 Ⓕ	Connectors				
Q103	B-3 Ⓕ	QR101	B-3 Ⓕ	IC204	C-4 Ⓕ	TG114	C-1 Ⓒ	P600	A-4 Ⓒ			
Q104	B-3 Ⓕ	QR102	B-3 Ⓕ	IC205	C-3 Ⓒ	TG300	E-2 Ⓕ	P601	A-4 Ⓒ			
Q105	C-3 Ⓕ	QR106	B-4 Ⓕ	IC301	C-1 Ⓒ			P602	A-3 Ⓒ			
Q106	A-3 Ⓕ	QR149	B-4 Ⓕ	IC302	B-1 Ⓒ			P603	A-3 Ⓒ			
Q301	D-2 Ⓕ	QR150	A-3 Ⓕ	IC303	D-1 Ⓕ			P604	A-3 Ⓒ			
Q302	D-2 Ⓕ	QR501	C-2 Ⓕ	IC401	A-1 Ⓕ			P605	A-2 Ⓒ			
Q401	A-3 Ⓒ	QR701	A-4 Ⓕ	IC402				P606	C-1 Ⓒ			
Q702	B-4 Ⓕ	QR702	A-4 Ⓕ	IC403	A-2 Ⓕ			P607	C-1 Ⓒ			
Q703	A-4 Ⓒ	QR703	B-4 Ⓕ	IC404	A-1 Ⓕ			P608	D-2 Ⓒ			
Q811	D-3 Ⓒ	QR801	D-1 Ⓕ	IC405	E-2 Ⓕ			P609	E-3 Ⓒ			
Q812	D-4 Ⓕ	QR804	D-1 Ⓕ	IC406	A-4 Ⓕ			P610	D-3 Ⓒ			
Q815	A-3 Ⓕ	QR809	D-1 Ⓕ	IC407	A-3 Ⓒ			P611	E-4 Ⓒ			
Q816	A-3 Ⓕ	QR810	E-1 Ⓕ	IC409	A-1 Ⓕ			P612	D-4 Ⓒ			
Q817	B-2 Ⓕ	QR813	E-1 Ⓕ	IC410	E-1 Ⓕ			P613	B-4 Ⓒ			
Q819	A-2 Ⓕ	QR814	A-3 Ⓕ	IC502	C-2 Ⓕ			P614	A-1 Ⓒ			
Q820	A-2 Ⓕ	QR818	A-2 Ⓕ	IC503	C-1 Ⓕ			P615	E-1 Ⓒ			
Q821	A-1 Ⓕ	QR824	E-2 Ⓕ	IC701	A-4 Ⓒ			P616	C-4 Ⓒ			
Q822	A-3 Ⓕ	QR828	D-2 Ⓕ	IC702	E-4 Ⓕ			P617	D-4 Ⓒ			
Q823	A-3 Ⓕ	QR834	E-3 Ⓒ	IC801	D-1 Ⓕ			P618	B-4 Ⓒ			
Q825	D-2 Ⓕ	QR838	E-3 Ⓕ	IC802	D-4 Ⓕ			P619	B-4 Ⓒ			
Q826	E-2 Ⓕ	QR844	E-2 Ⓕ	IC803	D-1 Ⓕ			P620	B-1 Ⓒ			
Q827	D-3 Ⓕ	QR845	E-2 Ⓕ	IC804	D-2 Ⓒ			P621	C-1 Ⓒ			
Q829	D-2 Ⓕ	QR846	E-2 Ⓕ	IC805	D-1 Ⓒ							
Q830	D-2 Ⓒ	QR905	B-2 Ⓕ	IC806	D-2 Ⓕ							
Q831	D-3 Ⓕ	QR907	B-2 Ⓕ	Test Points								
Q832	E-2 Ⓕ	QR913	B-1 Ⓕ	TP100	B-1 Ⓒ							
Q833	E-3 Ⓕ	QR915	B-2 Ⓕ	TP101	E-3 Ⓕ							
Q835	D-3 Ⓒ	QR917	B-2 Ⓕ	TP102	A-2 Ⓕ							
Q836	D-3 Ⓕ	QR919	B-4 Ⓒ	TP107	A-4 Ⓕ							
Q837	E-3 Ⓕ	QR920	B-4 Ⓒ	TP113	A-2 Ⓕ							
Q839	E-3 Ⓕ	QR921	B-3 Ⓕ	TP115	A-3 Ⓕ							
Q840	E-3 Ⓒ	Integrated Circuit		TP116	E-3 Ⓕ							
Q841	E-3 Ⓕ	IC6	C-4 Ⓕ	TP201	E-4 Ⓕ							
Q842	D-3 Ⓕ	IC7	B-4 Ⓕ	TP301	B-1 Ⓕ							
Q843	D-3 Ⓕ	IC9	C-2 Ⓕ	TP302	C-1 Ⓕ							
				TP402	A-2 Ⓕ							

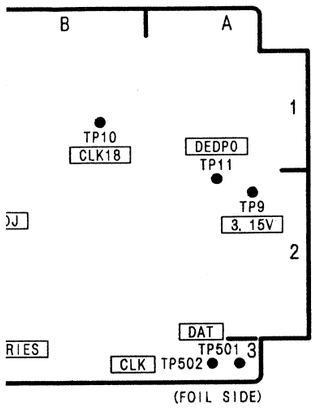
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

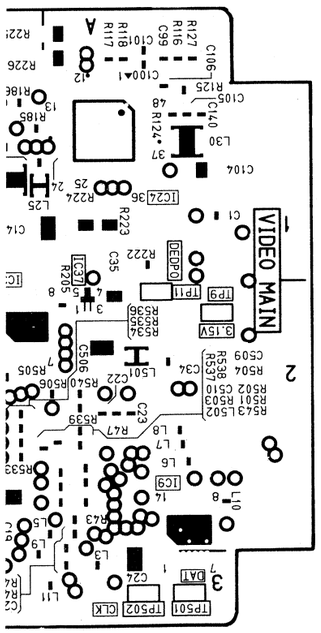
VIDEO MAIN P.C. BOARD (VEP03B96A)

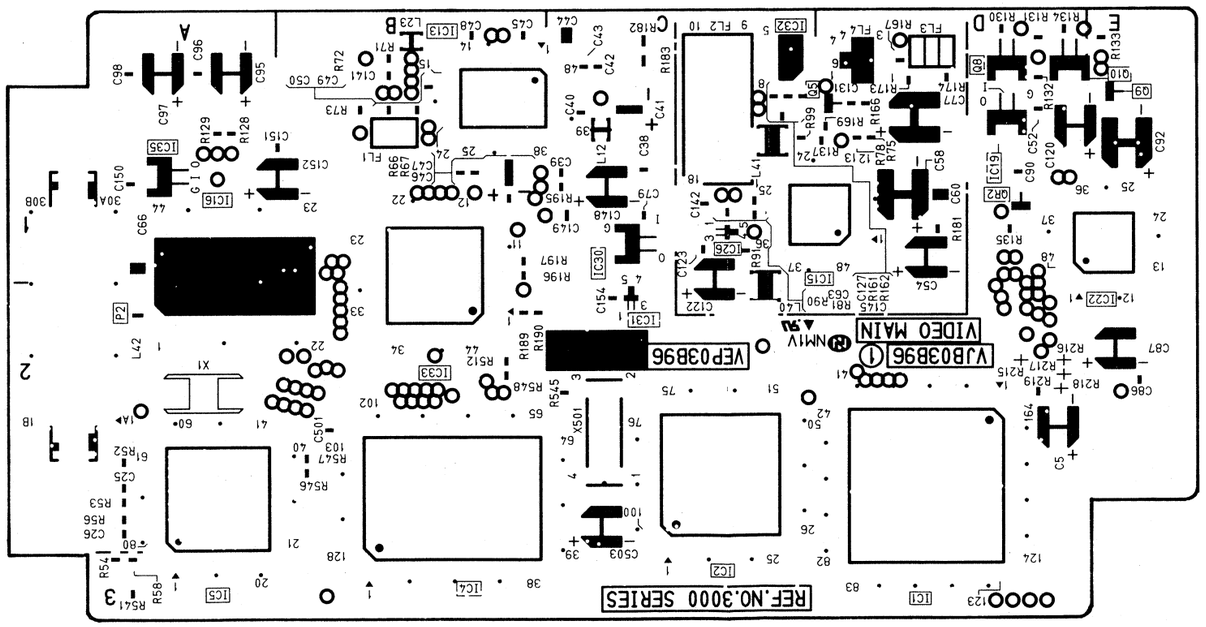












VIDEO MAIN	
Transistors	
Q1	C-1 Ⓕ
Q2	C-1 Ⓕ
Q3	C-1 Ⓕ
Q4	C-1 Ⓕ
Q5	C-1 Ⓒ
Q6	D-1 Ⓕ
Q7	D-1 Ⓕ
Q8	D-1 Ⓒ
Q9	E-1 Ⓒ
Q10	E-1 Ⓒ
Q11	C-1 Ⓕ
Q12	D-2 Ⓕ
Q13	D-2 Ⓕ
Transistor-Resistors	
QR1	D-2 Ⓕ
QR2	D-1 Ⓒ
Integrated Circuit	
IC1	D-3 Ⓒ
IC2	C-3 Ⓒ
IC3	C-3 Ⓕ
IC4	B-3 Ⓒ
IC5	A-3 Ⓒ
IC6	D-2 Ⓕ
IC7	C-3 Ⓕ
IC9	A-2 Ⓕ
IC10	B-3 Ⓕ
IC11	B-1 Ⓕ
IC12	C-1 Ⓕ
IC13	B-1 Ⓒ
IC14	C-2 Ⓕ
IC15	D-1 Ⓒ
IC16	A-1 Ⓒ
IC19	D-1 Ⓒ
IC20	D-1 Ⓕ
IC22	E-2 Ⓒ
IC23	E-1 Ⓕ
IC24	A-1 Ⓕ
IC25	D-2 Ⓕ
IC26	C-1 Ⓒ
IC30	C-1 Ⓒ
IC32	C-1 Ⓕ
IC33	B-2 Ⓒ
IC35	A-1 Ⓕ
IC36	B-2 Ⓕ
IC37	A-1 Ⓕ
IC501	B-2 Ⓕ
IC502	C-2 Ⓕ
IC503	B-1 Ⓕ
Test Points	
TP1	D-3 Ⓕ
TP2	D-3 Ⓕ
TP3	C-2 Ⓕ
TP4	D-1 Ⓕ
TP5	D-1 Ⓕ
TP6	D-2 Ⓕ
TP7	C-1 Ⓕ
TP8	B-2 Ⓕ
TP9	A-2 Ⓕ
TP10	B-1 Ⓕ
TP11	A-2 Ⓕ
TP501	A-3 Ⓕ
TP502	A-3 Ⓕ
Adjustments	
VR5	C-1 Ⓕ
VR6	C-1 Ⓕ
VR7	C-1 Ⓕ
Connectors	
P1	E-2 Ⓕ
P2	A-2 Ⓒ
P3	D-1 Ⓕ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

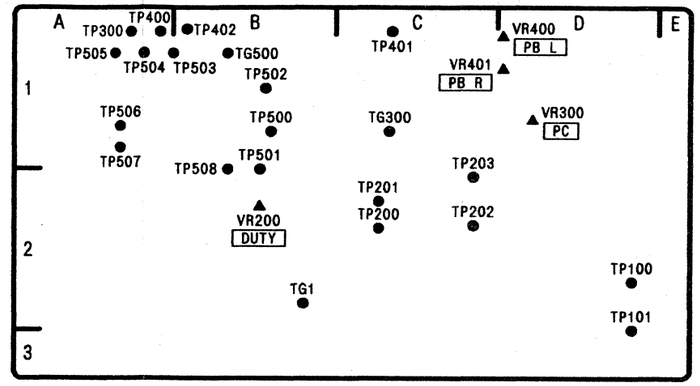
RF P.C. BOARD (VEP03B95A)

RF

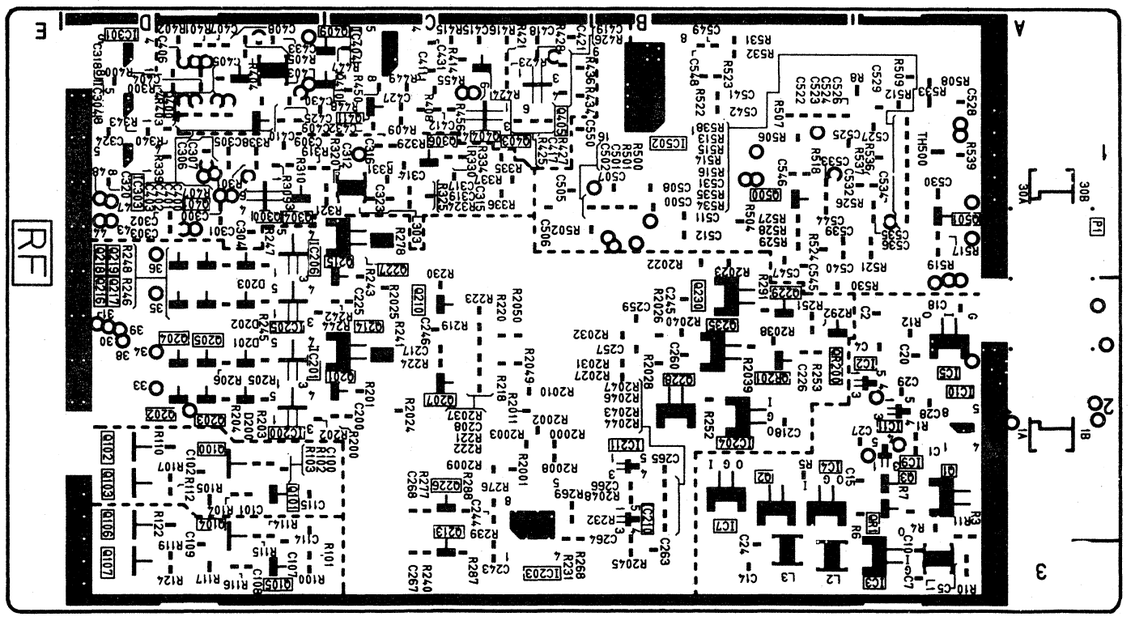
Transistors		
Q1	A-2	Ⓕ
Q2	B-2	Ⓕ
Q3	A-2	Ⓒ
Q100	D-2	Ⓕ
Q101	D-2	Ⓕ
Q102	D-2	Ⓕ
Q103	D-2	Ⓕ
Q104	D-2	Ⓕ
Q105	D-2	Ⓕ
Q106	D-2	Ⓕ
Q107	D-3	Ⓕ
Q201	C-2	Ⓕ
Q202	D-2	Ⓕ
Q203	D-2	Ⓕ
Q204	D-2	Ⓕ
Q205	D-2	Ⓕ
Q207	C-2	Ⓕ
Q208	D-2	Ⓒ
Q209	D-2	Ⓒ
Q210	C-2	Ⓕ
Q211		
Q212	C-3	Ⓒ
Q213	C-2	Ⓕ
Q214	C-2	Ⓕ
Q215	C-1	Ⓕ
Q216	D-2	Ⓕ
Q217	D-2	Ⓕ
Q218	D-1	Ⓕ
Q219	D-1	Ⓕ
Q221	D-2	Ⓒ
Q222	D-1	Ⓒ
Q224		
Q225	C-2	Ⓒ
Q226	C-2	Ⓕ
Q227	C-1	Ⓕ
Q228	B-2	Ⓕ
Q229	B-2	Ⓕ
Q230	B-2	Ⓕ
Q231	C-2	Ⓒ
Q232	C-2	Ⓒ
Q233	C-2	Ⓒ
Q234	C-1	Ⓒ
Q235	B-2	Ⓕ
Q300	D-1	Ⓕ
Q304	D-1	Ⓕ
Q305	C-1	Ⓒ
Q306	C-1	Ⓕ
Q307	C-1	Ⓒ
Q400	D-1	Ⓕ
Q401	D-1	Ⓕ
Q403	C-1	Ⓕ
Q404	C-1	Ⓕ
Q405	C-1	Ⓕ
Q406	B-1	Ⓒ
Q407	B-1	Ⓒ
Q408	B-2	Ⓒ
Q409	C-1	Ⓕ
Q410	C-1	Ⓕ
Q411	C-1	Ⓕ
Q500	B-1	Ⓕ
Q501	A-1	Ⓕ
Transistor-Resistors		
QR1	A-2	Ⓒ
QR100	D-2	Ⓒ
QR101	D-3	Ⓒ
QR200	B-2	Ⓕ
QR201	B-2	Ⓕ
QR400	C-1	Ⓒ
QR401	B-1	Ⓒ
Integrated Circuit		
IC1	B-2	Ⓒ
IC2	A-2	Ⓕ
IC3	A-3	Ⓕ
IC4	B-2	Ⓕ
IC5	A-2	Ⓕ
IC6	A-2	Ⓒ
IC7	B-2	Ⓕ
IC100	D-3	Ⓒ
IC101	D-2	Ⓒ
IC200	D-2	Ⓕ
IC201	D-2	Ⓕ
IC203	C-3	Ⓕ
IC204	B-2	Ⓕ
IC205	D-2	Ⓕ
IC206	D-1	Ⓕ
IC207	C-2	Ⓒ
IC208	B-2	Ⓒ
IC300	D-1	Ⓒ
IC301	D-1	Ⓕ
IC302	C-1	Ⓒ
IC303	D-1	Ⓕ
IC304	D-1	Ⓕ
IC400	D-1	Ⓒ
IC401	C-1	Ⓒ
IC402	C-1	Ⓒ
IC403	D-1	Ⓒ
IC404	B-1	Ⓕ
IC500	C-2	Ⓒ
IC501	A-1	Ⓒ
IC502	B-1	Ⓕ
Test Points		
TP100	D-2	Ⓒ
TP101	D-2	Ⓒ
TP200	C-2	Ⓒ
TP201	C-2	Ⓒ
TP202	C-2	Ⓒ
TP203	C-2	Ⓒ
TP300	A-1	Ⓒ
TP400	A-1	Ⓒ
TP401	C-1	Ⓒ
TP402	A-1	Ⓒ
TP500	B-1	Ⓒ
TP501	B-2	Ⓒ
TP502	B-1	Ⓒ
TP503	A-1	Ⓒ
TP504	A-1	Ⓒ
TP505	A-1	Ⓒ
TP506	A-1	Ⓒ
TP507	A-1	Ⓒ
TP508	B-2	Ⓒ
TG1	B-1	Ⓒ
TG300	C-1	Ⓒ
TG500	B-1	Ⓒ
Adjustments		
VR200	B-2	Ⓒ
VR400	C-1	Ⓒ
VR401	C-1	Ⓒ
Connectors		
P1	A-1	Ⓕ
P2	A-2	Ⓒ
P3	D-2	Ⓒ
P4	D-1	Ⓒ

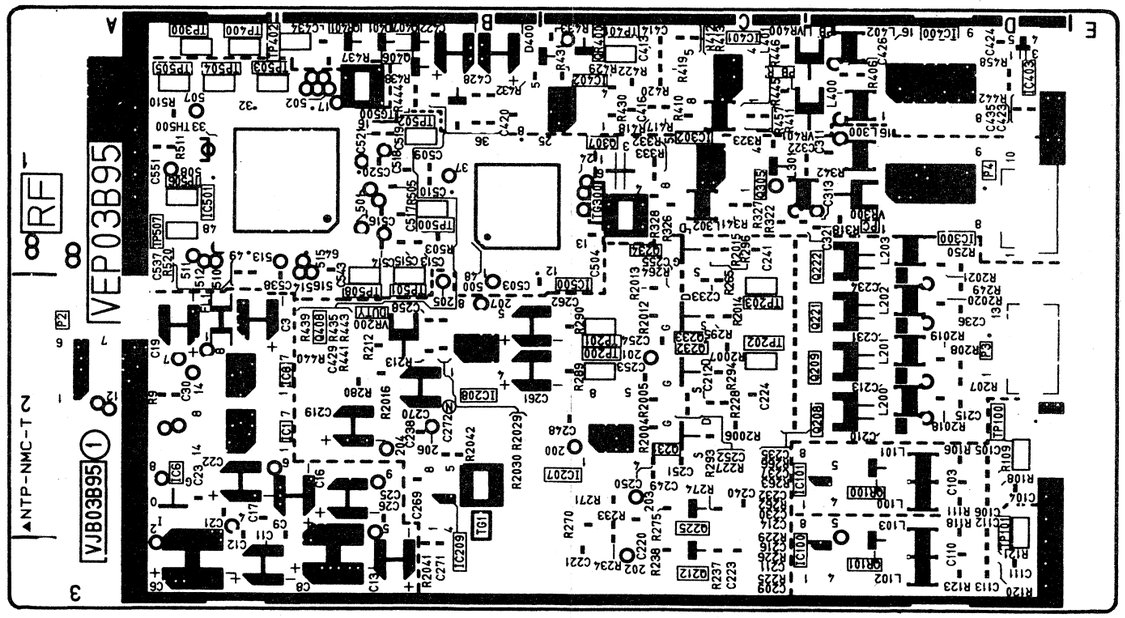
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

RF P. C. BOARD

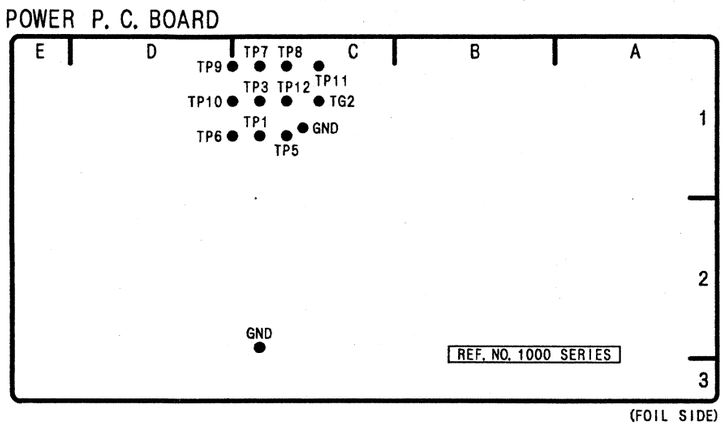


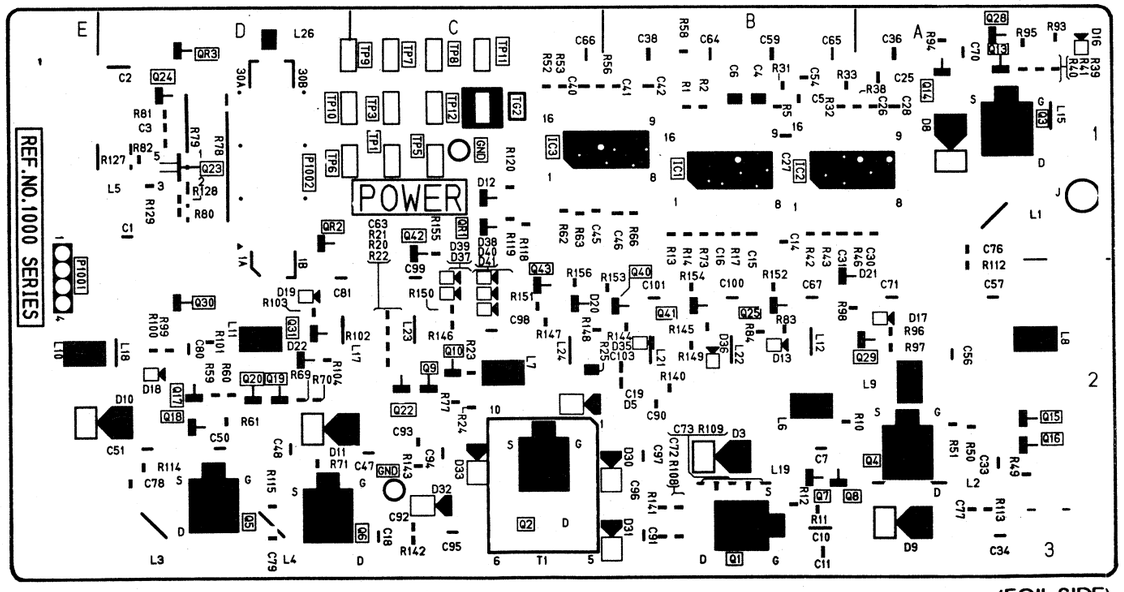
(COMPONENT SIDE)

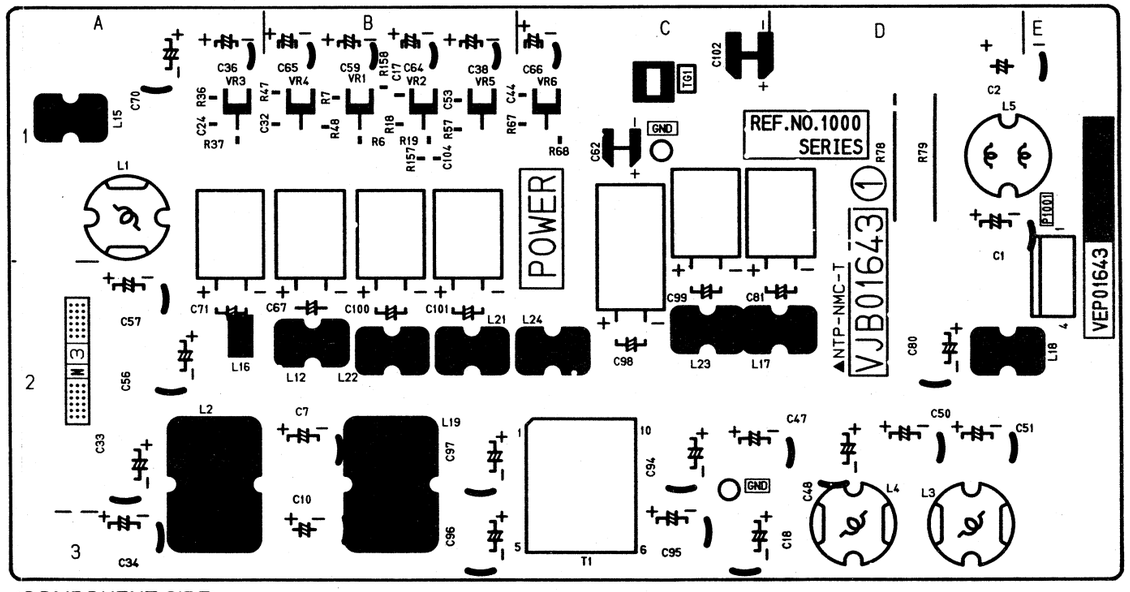




POWER P.C. BOARD (VEP01643A)







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POWER

Transistors

Q1001	B-3	Ⓕ
Q1002	C-3	Ⓕ
Q1003	A-1	Ⓕ
Q1004	A-2	Ⓕ
Q1005	D-3	Ⓕ
Q1006	C-3	Ⓕ
Q1007	B-2	Ⓕ
Q1008	B-2	Ⓕ
Q1009	C-2	Ⓕ
Q1010	C-2	Ⓕ
Q1013	A-1	Ⓕ
Q1014	A-1	Ⓕ
Q1015	A-2	Ⓕ
Q1016	A-2	Ⓕ
Q1017	D-2	Ⓕ
Q1018	D-2	Ⓕ
Q1019	D-2	Ⓕ
Q1020	D-2	Ⓕ
Q1022	C-2	Ⓕ
Q1023	D-1	Ⓕ
Q1024	D-1	Ⓕ
Q1025	B-2	Ⓕ
Q1028	A-1	Ⓕ
Q1029	A-2	Ⓕ
Q1030	D-2	Ⓕ
Q1031	D-2	Ⓕ
Q1040	B-2	Ⓕ
Q1041	B-2	Ⓕ
Q1042	C-1	Ⓕ
Q1043	C-2	Ⓕ

Transistor-Resistors

QR1001	C-1	Ⓕ
QR1002	D-1	Ⓕ
QR1003	D-1	Ⓕ

Integrated Circuit

IC1001	C-1	Ⓕ
IC1002	B-1	Ⓕ
IC1003	B-1	Ⓕ

Test Points

TP1	C-1	Ⓕ
TP3	C-1	Ⓕ
TP5	C-1	Ⓕ
TP6	D-1	Ⓕ
TP7	C-1	Ⓕ
TP8	C-1	Ⓕ
TP9	C-1	Ⓕ
TP10	D-1	Ⓕ
TP11	C-1	Ⓕ
TP12	C-1	Ⓕ
TG1001	C-1	Ⓒ
TG1002	C-1	Ⓕ

Adjustments

VR1001	B-1	Ⓒ
VR1002	B-1	Ⓒ
VR1003	A-1	Ⓒ
VR1004	B-1	Ⓒ
VR1005	B-1	Ⓒ
VR1006	C-1	Ⓒ

Connectors

P1001	E-1	
P1002	D-1	Ⓕ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

AUDIO LCD

Transistors

Q4001	C-2	Ⓕ
Q4002	A-4	Ⓕ
Q4003	A-4	Ⓕ
Q4004	C-1	Ⓒ
Q4007	B-1	Ⓒ
Q4008	A-2	Ⓕ
Q4009	A-2	Ⓕ
Q4010	A-1	Ⓕ
Q4101	D-4	Ⓕ
Q4102	D-4	Ⓒ
Q4103	D-4	Ⓒ
Q4107	D-2	Ⓕ
Q4110	A-2	Ⓕ
Q4111	B-2	Ⓕ
Q4201	C-4	Ⓕ
Q4202	C-3	Ⓒ
Q4203	C-3	Ⓒ
Q4207	D-2	Ⓕ
Q4210	A-2	Ⓕ
Q4211	A-2	Ⓕ
Q4302	B-4	Ⓕ
Q4305	C-4	Ⓕ
Q4306	D-4	Ⓕ
Q4307	D-4	Ⓕ
Q4402	A-4	Ⓕ
Q4405	C-3	Ⓕ
Q4406	C-3	Ⓕ
Q4407	C-4	Ⓕ
Q4702	B-3	Ⓕ
Q4703	A-3	Ⓕ
Q4704	B-3	Ⓒ
Q4705	B-3	Ⓒ
Q6501	E-3	Ⓕ
Q6502	E-3	Ⓕ
Q6503	F-1	Ⓕ

Transistor-Resistors

QR4001	A-2	Ⓕ
QR4006	A-1	Ⓕ
QR4007	A-1	Ⓕ
QR4010	D-1	Ⓕ
QR4012	B-1	Ⓒ
QR4013	B-1	Ⓕ
QR4102	D-2	Ⓕ
QR4103	B-1	Ⓕ
QR4104	B-1	Ⓕ
QR4105	B-2	Ⓕ
QR4106	B-2	Ⓕ
QR4107	B-1	Ⓕ
QR4108	B-1	Ⓕ
QR4201	D-2	Ⓕ
QR4202	D-2	Ⓕ
QR4203	A-3	Ⓕ
QR4204	A-3	Ⓕ
QR4205	A-3	Ⓕ
QR4206	B-2	Ⓕ
QR4207	A-1	Ⓕ
QR4208	A-1	Ⓕ
QR4301	D-4	Ⓕ
QR4302	D-4	Ⓕ
QR4303	D-4	Ⓕ
QR4304	C-4	Ⓕ
QR4401	D-4	Ⓕ
QR4402	D-4	Ⓕ
QR4403	C-4	Ⓕ
QR4404	C-4	Ⓕ
QR4507	B-3	Ⓕ
QR4508	C-2	Ⓕ
QR4601	F-1	Ⓕ
QR6501	G-1	Ⓕ
QR6502	G-2	Ⓕ
QR6503	F-1	Ⓕ
QR6504	F-1	Ⓕ

Integrated Circuits

IC4001	B-2	Ⓒ
IC4002	C-2	Ⓕ
IC4003	E-1	Ⓕ
IC4004	B-2	Ⓕ
IC4005	D-3	Ⓕ
IC4006	C-1	Ⓕ
IC4007	D-1	Ⓒ
IC4008	D-1	Ⓒ
IC4009	C-2	Ⓕ
IC4010	C-1	Ⓕ
IC4011	B-1	Ⓕ
IC4012	B-1	Ⓕ
IC4013	A-1	Ⓕ
IC4014	D-1	Ⓒ
IC4015	C-2	Ⓕ
IC4016	D-2	Ⓕ
IC4017	B-4	Ⓕ
IC4102	D-2	Ⓕ
IC4103	D-4	Ⓕ
IC4105	D-3	Ⓕ
IC4202	D-2	Ⓕ
IC4203	D-3	Ⓕ
IC4205	C-3	Ⓕ
IC4501	C-2	Ⓕ
IC4502	B-4	Ⓕ
IC4503	C-3	Ⓒ
IC4602	E-2	Ⓕ
IC4603	E-2	Ⓕ
IC4701	B-3	Ⓕ
IC4702	B-3	Ⓕ
IC4703	C-4	Ⓒ
IC4704	A-2	Ⓕ
IC6501	F-1	Ⓕ
IC6502	G-3	Ⓕ
IC6503	E-3	Ⓕ
IC6505	G-4	Ⓕ

Test Points

TP4101	D-1	Ⓕ
TP4102	E-2	Ⓕ
TP4201	D-1	Ⓕ
TP4202	E-2	Ⓕ
TP4501	B-3	Ⓕ
TP4505	C-2	Ⓕ
TP4601	F-2	Ⓕ
TP4602	F-1	Ⓕ
TP6501	E-3	Ⓕ
TP6502	G-1	Ⓕ
TP6503	G-1	Ⓕ
TP6504	G-1	Ⓕ
TP6505	F-1	Ⓕ
TP6506	F-1	Ⓕ
TG4001	D-2	Ⓕ

Adjustments

VR4001	C-1	Ⓕ
VR4002	C-1	Ⓕ
VR4101	F-3	
VR4102	D-3	
VR4103	C-2	
VR4201	F-3	
VR4202	C-3	
VR4203	D-2	
VR4301	B-3	
VR4401	B-4	
VR4501	C-3	
VR4503	C-4	Ⓕ
VR4701		

Switches

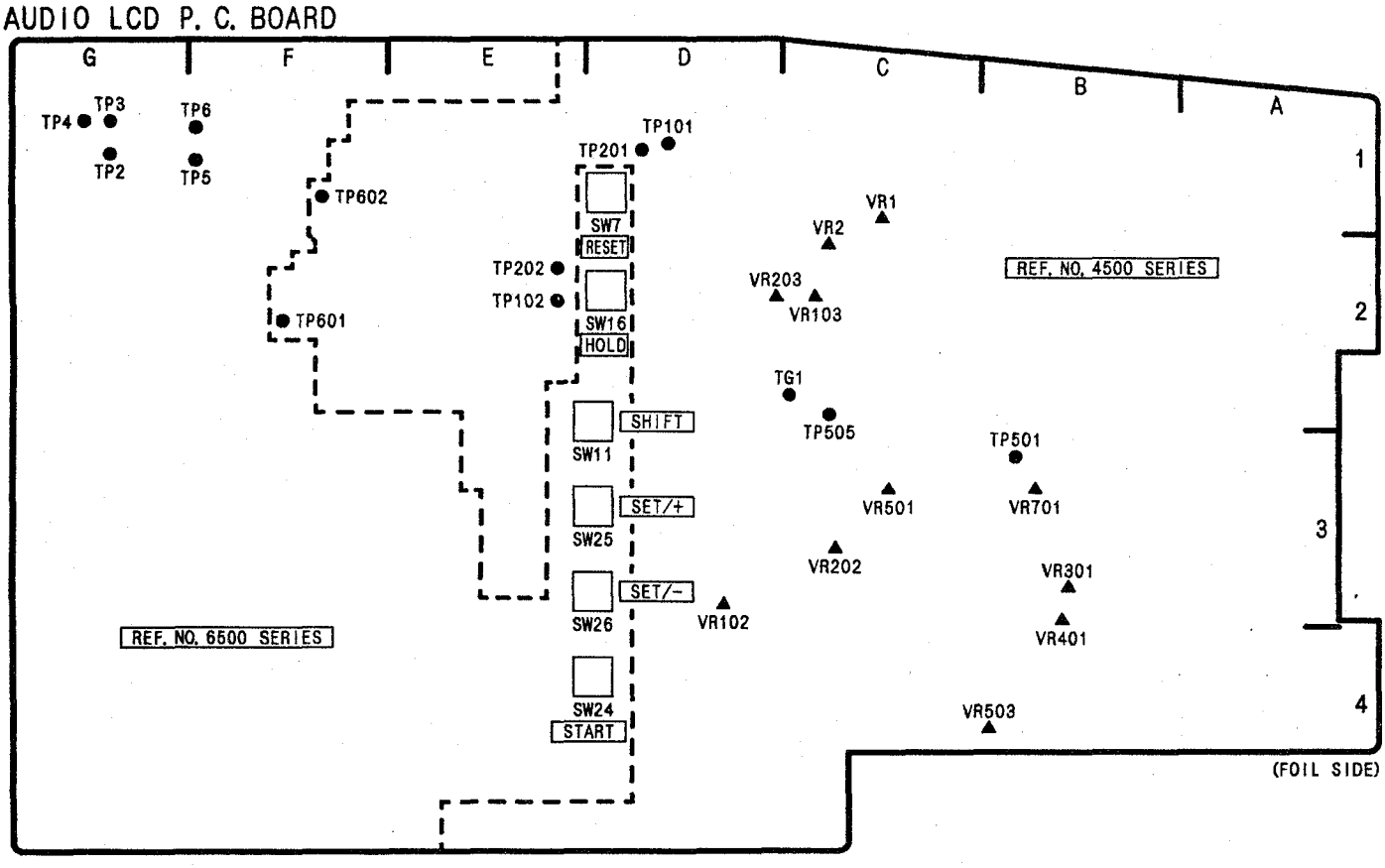
SW4701	G-1	Ⓒ
SW6501	G-1	
SW6502	G-1	
SW6503	E-4	
SW6504	G-2	
SW6505	G-3	
SW6506	G-4	
SW6507	D-1	
SW6508	F-3	
SW6509	F-3	
SW6510	E-3	
SW6511	D-3	
SW6512	F-4	
SW6514	F-4	
SW6516	D-2	
SW6524	D-4	
SW6525	D-3	
SW6526	D-3	

Connectors

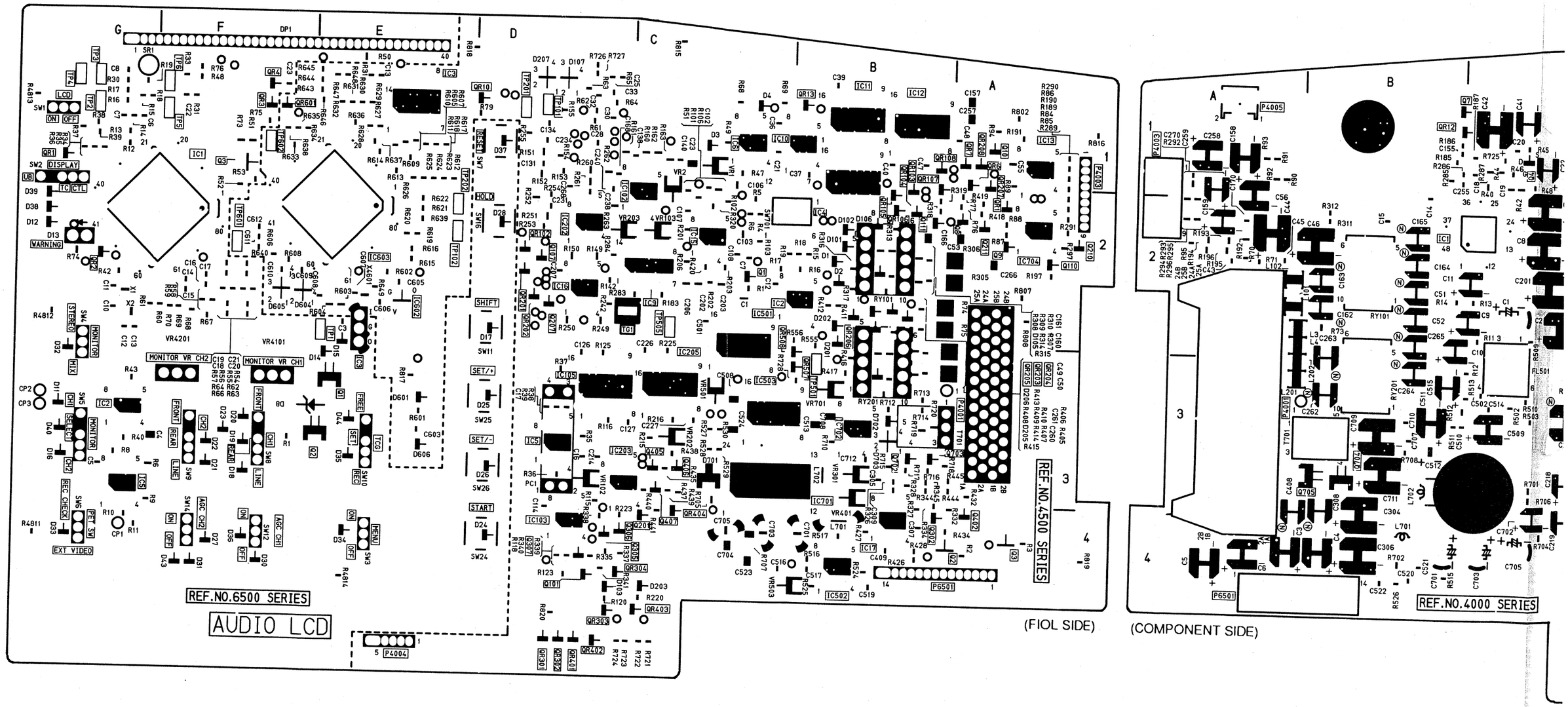
P4001	A-3	
P4002	G-4	Ⓒ
P4003	A-1	
P4004	E-4	
P4005	A-1	Ⓒ
P6501	A-4	

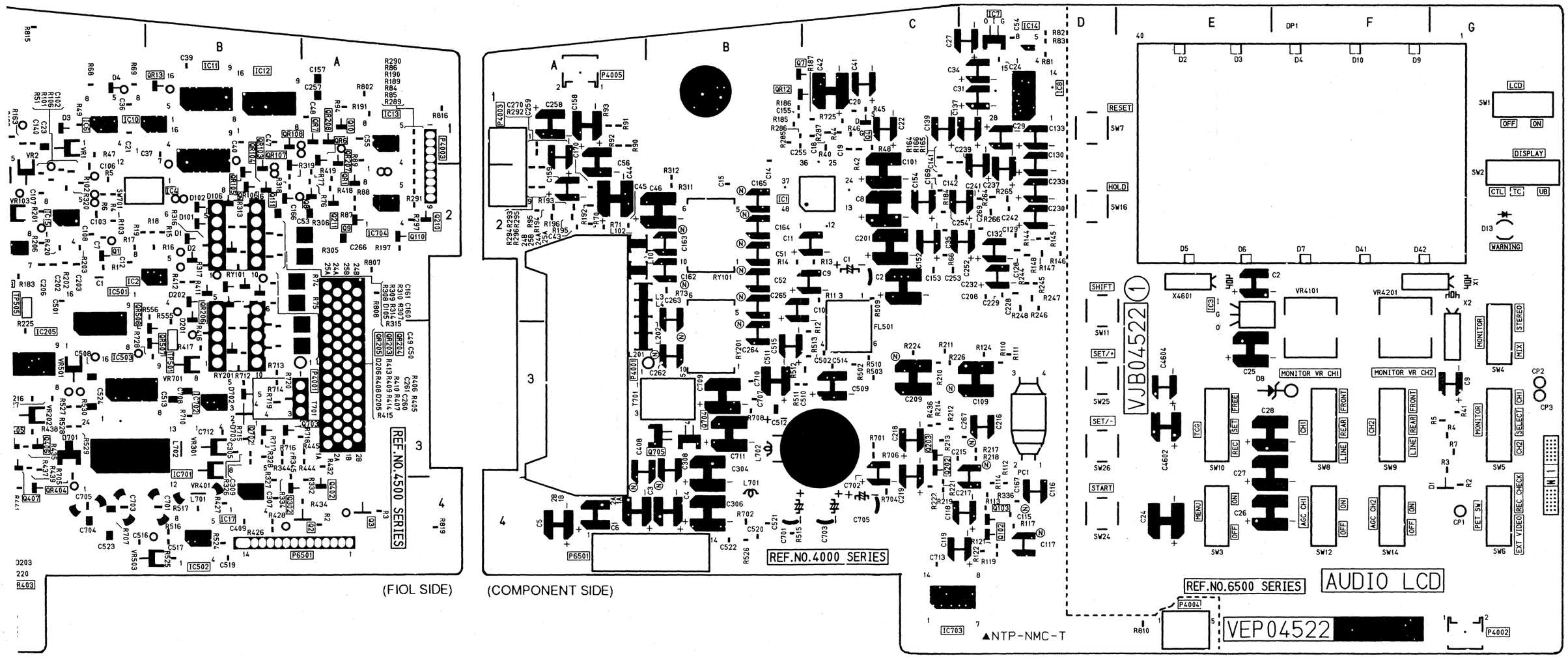
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

AUDIO LCD P. C. BOARD



AUDIO LCD P.C. BOARD (VEP04522A)




REF.NO.4500 SERIES
(FIOL SIDE)
REF.NO.4000 SERIES
(COMPONENT SIDE)
REF.NO.6500 SERIES
AUDIO LCD
VJB04522 1
VEP04522
▲NTP-NMC-T
RESET
SW7
HOLD
SW16
SHIFT
SW11
SET/+
SW25
SET/-
SW26
START
SW24
LCD
SW1
OFF
ON
DISPLAY
SW2
CTL
TC
UB
D13
WARNING
MONITOR VR CH1
MONITOR VR CH2
MONITOR
STEREO
MIX
SW4
SW10
SW8
SW9
SW5
SW3
SW12
SW14
SW6
REC
SEL
FREE
CH1
REAR
FRONT
LINE
CH2
MENU
OFF
ON
AGC CH1
AGC CH2
SELECT
REC CHECK
EXT VIDEO
PET SW
DP1
X4601
X1
X2
CP1
CP2
CP3

CIRCUIT BOARD LOCATION

Memo